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Borehole X-Ray Fluorescence Spectrometer (XRFS): User's Manual, Software Description, and Performance Report

built by APL-UW under a NASA contract from the Langley Research Center

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CAUTION CAUTION CAUTION

This device produces X-rays when energized.

CAUTION CAUTION CAUTION

Technical Report

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Contents

User's Manual 1
Overview 1
Borehole XRFS Software Installation 12
Instrument Design 15
Typical Operation 19
Determining the Minimum Detection Limit (MDL) 40
Hardware Description 23
XRF Interface Unit 23
XRF Control Unit 26
Software Description 29
X-ray Tube Control (XTC) 29
Detector Data Acquisition (DET) 31
Save and Load Parameters (PAR) 33
Save and Load Spectrum (SSF) 34
Spectrum Processing (SP) 36
Spectrum Display (SD) 36
Instrument Performance Report 38
Materials and Methods 39
Test Plan Summary 41
Results 42
Conclusions 52
Appendices 53

User's Manual

Overview

The X-ray fluorescence spectrometer (XRFS) is designed to be deployed down a pre-drilled hole for exploration and elemental analysis of subsurface planetary regolith (Figure 2 and Figure 10). The spectrometer excites atoms in the regolith and causes them to emit their characteristic X-rays. These characteristic X-rays produce peaks in the X-ray spectrum. By measuring the energy of the X-rays, elements are identified. By measuring the intensity of the peaks, the amount of each element can be determined. A software package operates the spectrometer, acquires the data, and analyzes the spectrum to provide elements and their weight fractions. It also provides a user interface to control the measurements and display the results.

Figure 1. X-ray fluorescence spectrometer **Head Unit** designed to be deployed down a pre-drilled hole to analyze subsurface elements.

The spectrometer consists of two main subsystems packaged in three physical units. The main subsystems are the X-ray source and the energy-dispersive X-ray detector. The source provides the X-rays to excite the specimen of regolith being investigated. The energy-dispersive X-ray detector detects the emitted X-rays, determines their energy (the energy-dispersive function), and counts the X-rays at each energy. Together these two subsystems measure the X-ray spectrum of the specimen.

Quick Start Guide

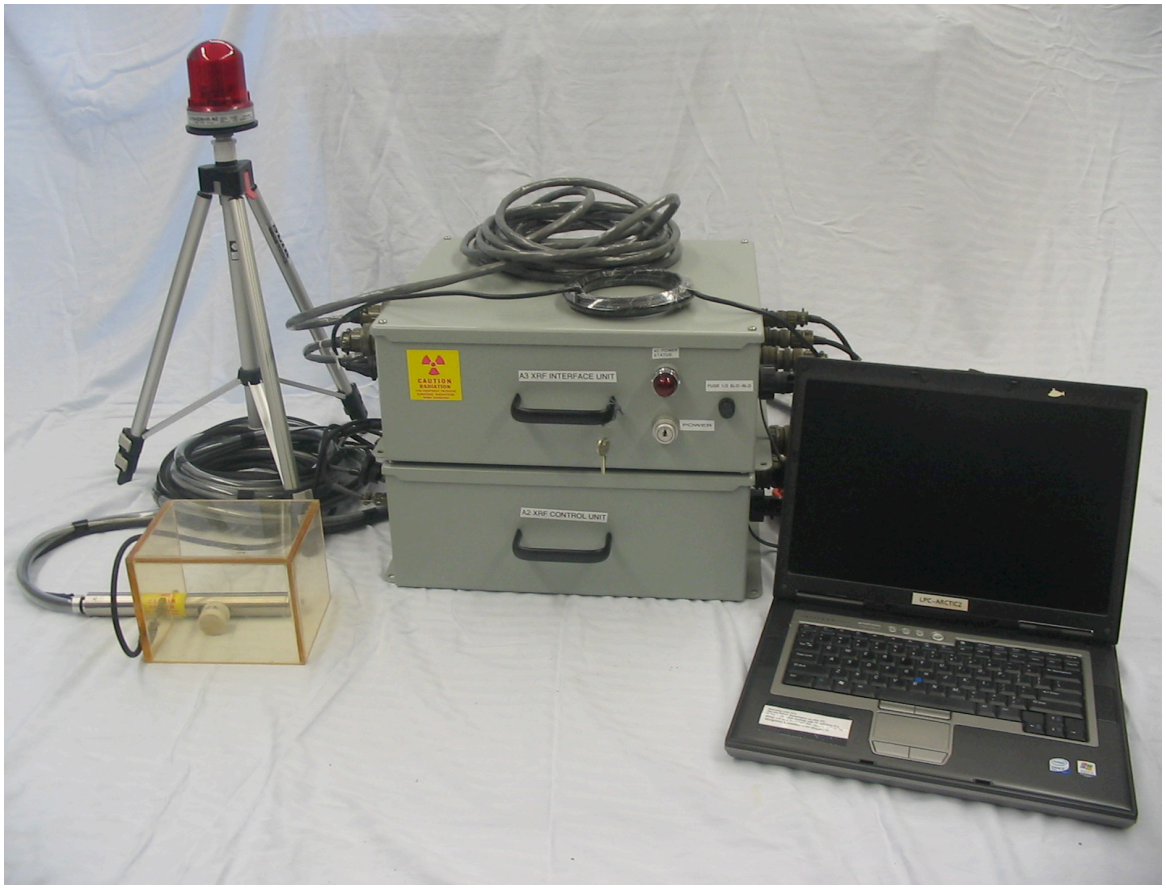

Figure 2. (from left to right) Borehole XRFS **Head Unit**, X-ray warning light, umbilical cable, X-ray **Interface** and **Control** units, and laptop computer.

Setup

To set up the instrument:

1. Remove the units from the case. The instrument consists of the **XRF Interface Unit**, the **XRF Control Unit**, and the **XRF Head Unit** (Figure 2). A laptop computer is used to control the instrument. There are three cables connecting the **Interface** and **Control** units, and the **Head Unit** has an umbilical cable (15 ft. long) permanently attached to connect it to the **Control Unit**. An X-ray warning light is also supplied. The instrument must be used in a radiation safety enclosure

or other personnel safety arrangement. An interlock cable connects to the safety interlock switch on the radiation safety enclosure to prevent accidental exposure.

2. Connect the cables as shown in Figure 3. All cables must be connected before turning on the main power.
3. Connect USB cable to the laptop computer and turn on the instrument with the key switch. The laptop should beep when it recognizes the connection to the instrument.
4. Wait one to two minutes for the detector to cool down. The instrument is now ready to collect a spectrum.

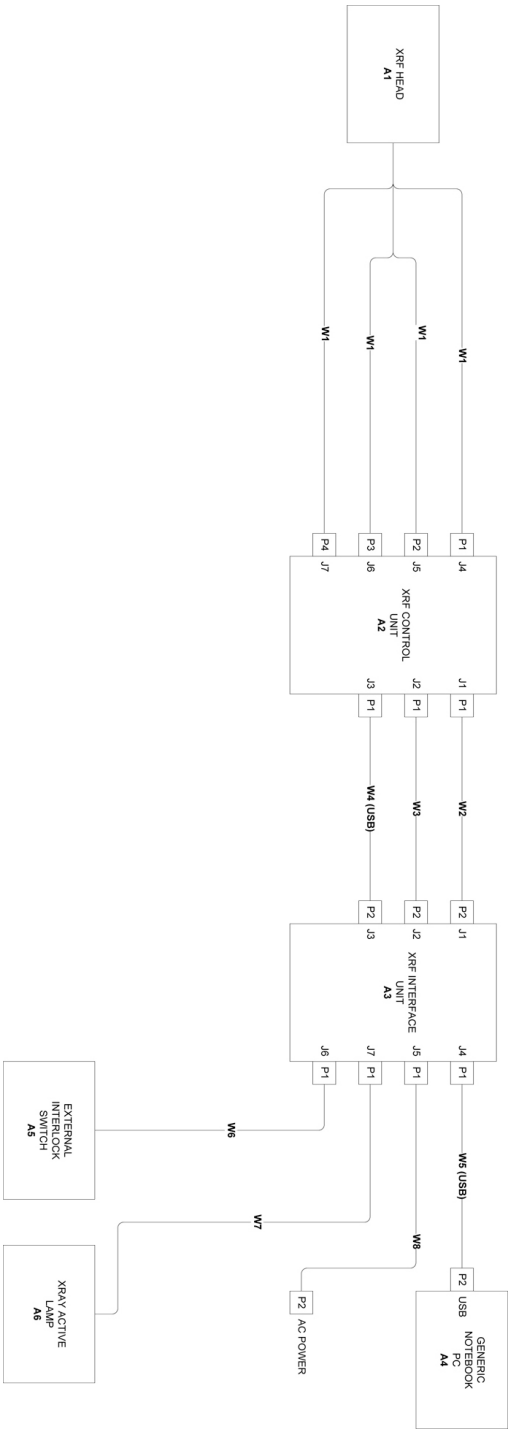

Figure 3. Connection diagrams for **Interface**, **Control**, and **Head** units of the XRF spectrometer.

Spectrum collection

1. Place the sample to be analyzed before the probe window.
2. Close the radiation safety enclosure and be sure the interlock switch is closed.
3. Start the program "BoreholeXRF"; the main screen appears (Figure 4).
4. Turn on the high voltage to 35 kV, and the emission current to 2 μA.
5. Set the preset time to the desired interval.
6. Click "Start".
7. The actual kV and μA values should be near the setting values (they may take one or two minutes to reach these values because of the slow ramp).
8. "Acquiring" will appear in red on the screen (Figure 5).
9. A spectrum will begin to appear in the plot box in the lower left corner of the interface (Figure 5).
10. To calibrate, click "Calibrate" and enter points in the form "channel number, energy in keV" in the window that opens (Figure 6). Then click "Compute," then "Calibrate," then "Close." You may calibrate before, during, or after spectrum collection.
11. To save the spectrum, click "Save."
12. To determine which elements are present in the sample, click the "Analyze" button. After several seconds, the plot box will show the background and spectrum fits and the elemental analysis will appear in the spectrum analysis box (Figure 7).

Software operation

Configuration settings:

- "load params panel" (Figure 8): Opening this window allows the user to change instrument control parameters (such as the ramp interval) and acquisition conditions (such as the atmosphere type).

- "load DP4 config panel" (Figure 9): Opening this panel allows the setting for the DP4 digital pulse processor to be changed. Refer to the AmpTek manual (Appendix A) on the DP4 for more information about these parameters.
- "on" and "off" under "X-ray control": These buttons turn the X-rays on and off.
- "setkV": This button allows the user to set the high voltage for the X-ray tube.
- "set μA": This button allows the user to set the emission current.
- "change preset time": Use this button to enter the desired interval of data collection in seconds, then click "OK." This command automatically clears the spectrum that is currently plotted (so save it first!). When the user clicks "Start" after entering this preset time, the program will collect a spectrum and stop automatically after the allotted time has elapsed. Note that this refers to accumulation time, not live time.

"Input Spectrum" functions:

- "Start": Click this button to begin taking a spectrum.
- "Stop": Click this button to stop spectrum collection before the preset time has elapsed.
- "Clear": This button clears the spectrum currently plotted.
- "Calibrate": The user may calibrate the energy of the spectrum any time before, during, or after collection. It is also possible to load and calibrate a previously saved spectrum. Click "Calibrate" to open the calibration window, enter the desired channel-energy pairs (in keV) in the form "channel, energy," click "Compute," "Calibrate," and "Close." It is also possible to type a desired energy-per-channel value and energy start value manually and then click "Calibrate," without pressing "Compute." The user may clear a previous calibration and return to the original channel values by pressing "Remove calibration."

- "Load": This button allows the user to bring up a previously saved spectrum. It is possible to enter a new spectrum label and operator, zoom in/out, calibrate, analyze and re-save any previously saved spectrum.

Plot controls: (Note: none of these buttons affect data collection.)

- "Restore": Restores the spectrum plot to its original scale and causes it to begin automatically adjusting the Y-scale to keep the entire spectrum in view.
- "← cursor": Moves the cursor one channel to the left.
- "cursor →": Moves the cursor one channel to the right.
- "X zoom in": Adjusts the X-scale so that it displays a smaller range of X values, centered around the cursor.
- "X zoom out": Adjusts the X-scale so that it displays a larger range of X values, centered around the cursor.
- "X shift left": Moves the view to the left approximately half of the plot range, so that the user is looking at slightly lower energies.
- "X shift right": Moves the view to the right approximately half of the plot range, so that the user is looking at slightly higher energies.
- "Y zoom in": Adjusts the Y-scale so that it displays a smaller range of Y values.
- "Y zoom out": Adjusts the Y-scale so that it displays a larger range of Y values.

"Analyze": Click this button (after calibrating) to run an automated analysis of the sample. It will return a list of elements present, their concentrations and uncertainty.

"Save spectrum": Allows the user to save the current spectrum and some configuration information to a file on the computer. These files are accessible by the "load" button in the Borehole XRF software, and can also be opened in a word processing program or text editor.

"Exit": Exits the spectrum collection program. The program will **not** prompt the user to save the current spectrum, so it is necessary to save (if desired) before exiting.

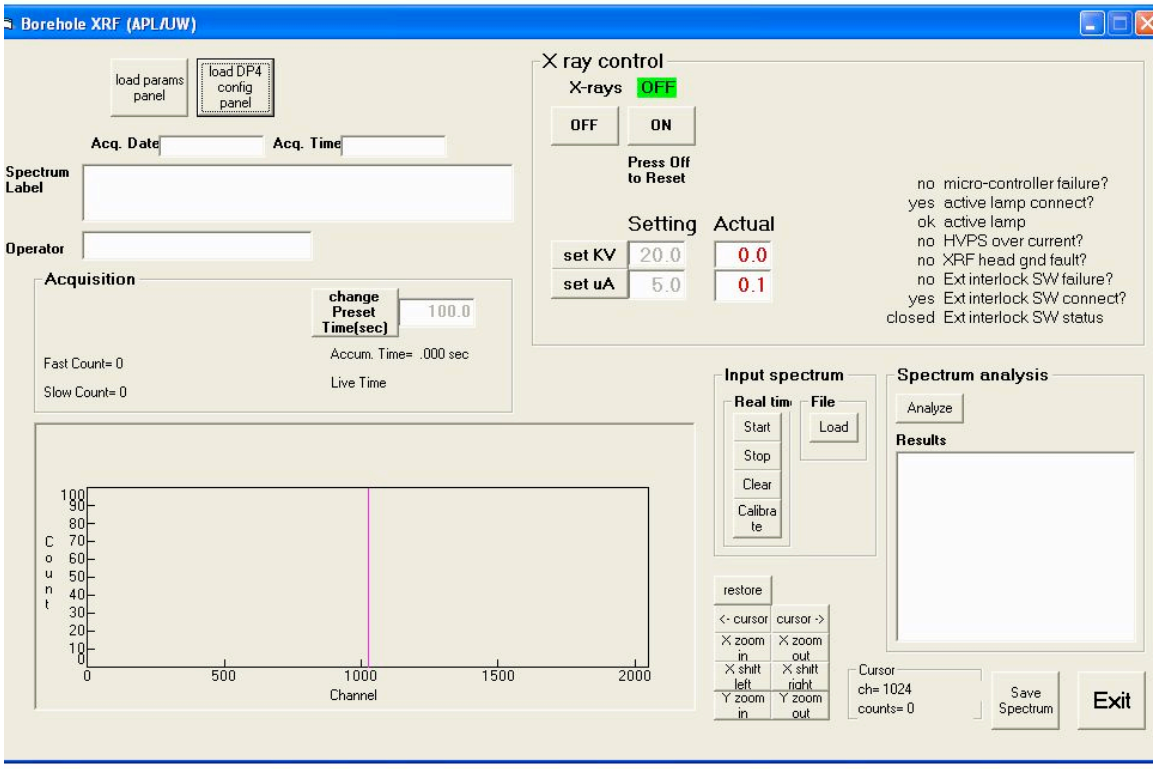

Figure 4. Main screen view upon starting the program "BoreholeXRF"

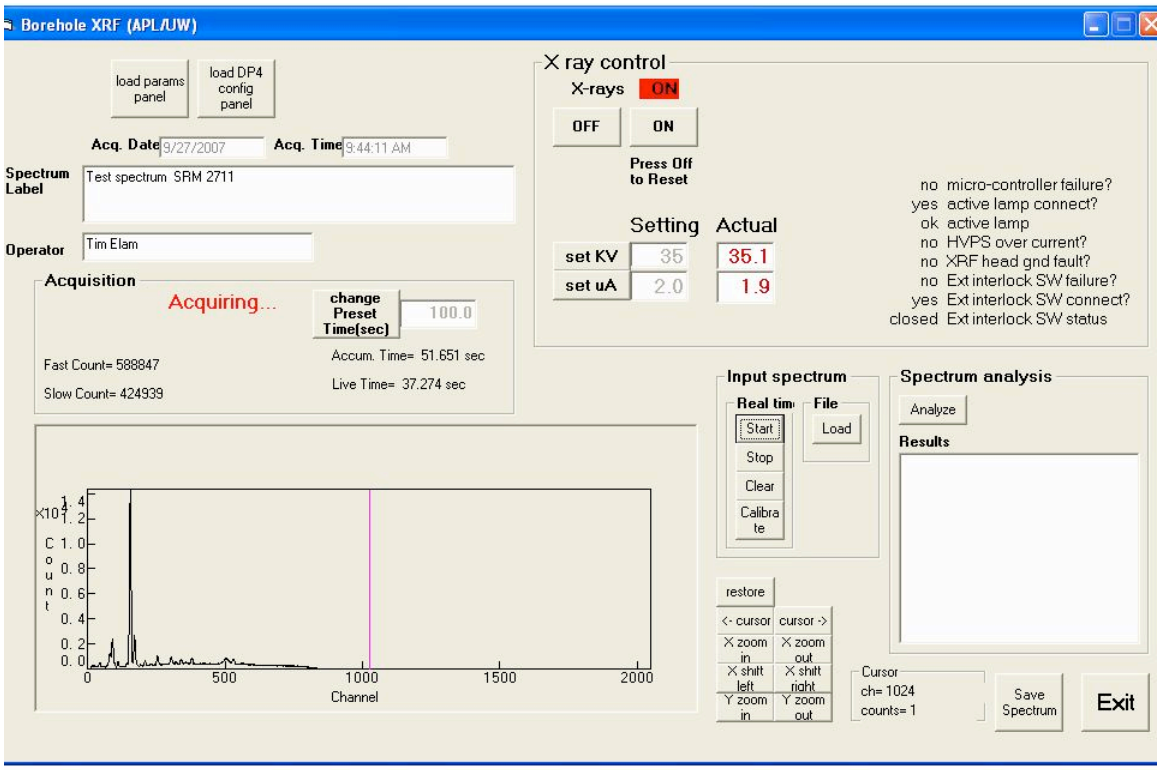

Figure 5. View of laptop display during spectrum acquisition

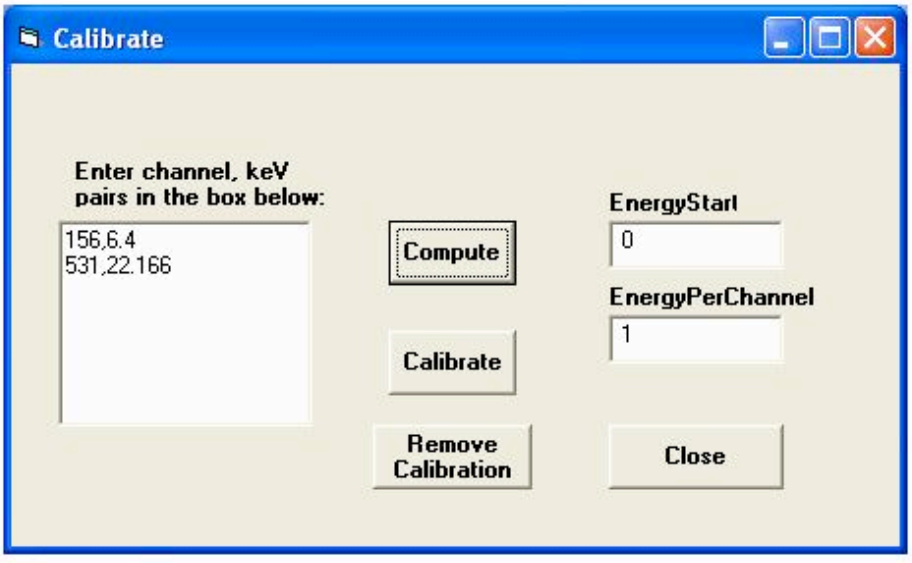

Figure 6. View of calibration control window

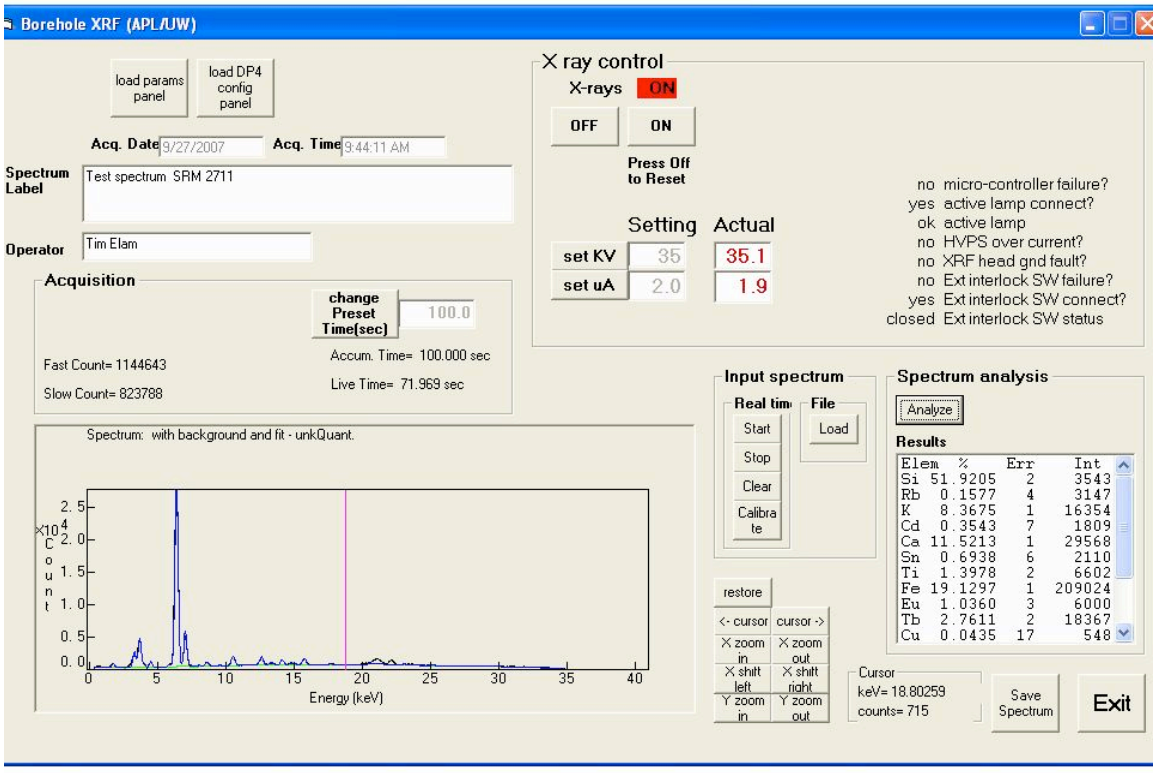

Figure 7. View of spectrum analysis display

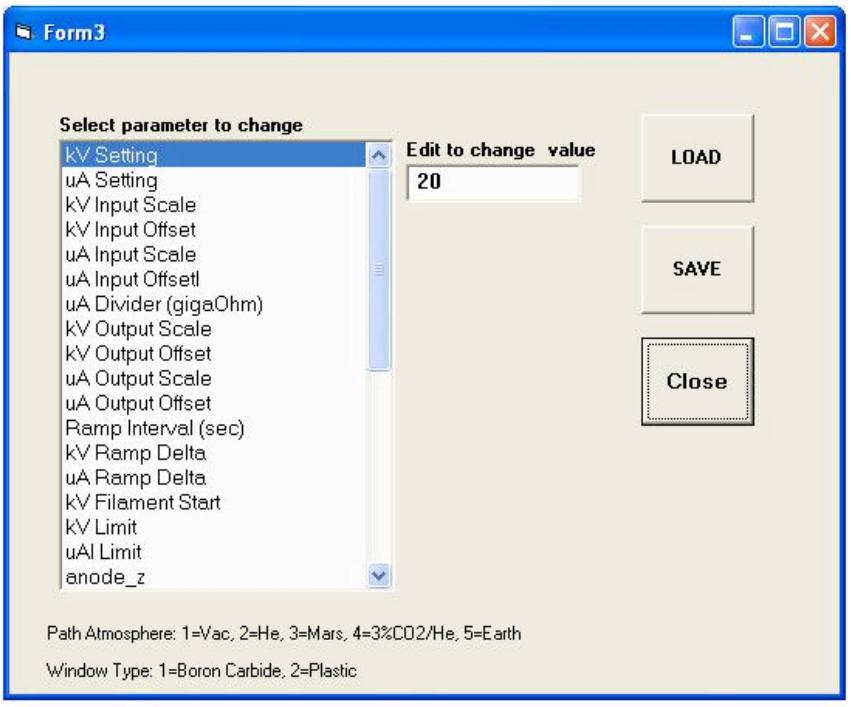

Figure 8. View of configuration setting “load parameters panel”

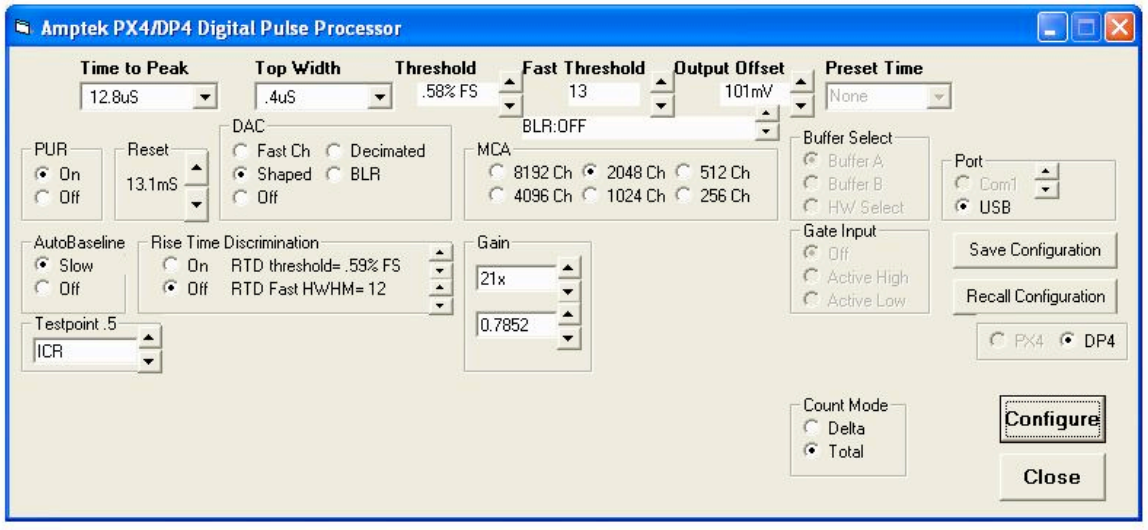

Figure 9. View of configuration setting “load DP4 configuration panel”

Borehole XRFS Software Installation

Before connecting hardware, copy all files from CD-R folder titled "BoreholeXRF As Shipped Bin Sept 27.2007."

Place files in C:\Program Files\BoreholeXRF

(Note: the files MUST be in exactly this location to operate correctly.)

Necessary software files from the folder "BoreholeXRF As Shipped Bin Sept 27.2007":

- xrayxsct.dat
- XRFanalysis.dll
- APL_UW_XraySettings.xcg
- asycfilt.dll
- BoreholeXRF.exe
- cbw32.dll
- COMCAT.DLL
- COMCT232.OCX
- Comdlg32.ocx
- dp4.cfg
- MSCOMM32.OCX
- msvbvm60.dll
- oleaut32.dll
- olepro32.dll
- usbdrvd.dll

Install the driver for the Measurement Computing DAQ module.

- Load the Measurement Computing "MCC DAQ Software" CD
- Install InstaCal for Windows, TracerDAQ, and Hadware manuals
- Install Shield Wizard for InstaCal – click "Next"
- Destination Folder – click "Next"

- Ready to Install – click “Install”
- Completed – click “Finish”
- Install Shield Wizard for TracerDAQ – click “Next”
- Destination Folder – click “Next”
- Ready to Install – click “Install”
- Completed – click “Finish”
- User's Guides Setup – select “USB,” then click “Install”
  (Driver is installed. This takes a few seconds.)
- MCC DAQ message box – “You must restart your system...” – click “Yes”

After system has restarted, connect Borehole XRF hardware to USB port and turn power on. “Found New Hardware Wizard” should appear.

“Can Windows connect to Windows Update...” – choose “No, not at this time.” – click “Next”

Install software for DP4 Digital Pulse Processor (see also page 19 of Appendix A)

- Select “Install from a list or specific location” – click “Next”
- Select “Don't search, I will choose the driver to install” – click “Next”
- Hardware type – Select “Human Interface Devices” – click “Next”
- “Select the device driver...” – Click “Have disk...”
- Insert the AmpTek CD into the CD drive
- Click “Browse...”
- “Install From Disk” file dialog appears
- Navigate in the file dialog to:
  My Computer\AMPTEK\USB_Driver\Win2k_XP\apausb2k.ini
- Click “Open”
- Back at the “Install From Disk” dialog – click “OK”
- Back to “Select the device driver...” dialog – click “Next”
  (Driver is installed. This takes a few seconds.)

- Completing installation – click “Finish”

Run the InstaCal program

- From the menu bar, select: Start -> Programs -> Measurement Computing -> Instacal
- “Plug and Play Board Detection, USB-1408FS (Serial# 150)” should be selected
- Click “OK”
- Under the Install menu item, choose “Configure...”
- Change No. of Channels from “4 Differential” to “8 Single Ended”
- Click “OK”
- Under the File menu item, choose “Exit”

Run the Borehole XRF program by double-clicking on the file “Borehole XRF.exe”

At this point the software main screen should appear; it will obtain a spectrum and bring up all dialogs.

You may want to put a shortcut to the “Borehole XRF.exe” file on the desktop or some other convenient location.

Instrument Design

The instrument is designed to be deployed down a pre-drilled borehole and has a maximum diameter of 27.1 mm to be compatible with existing drills (Figure 1 and Figure 10). The XRFS sensor assembly consists of an XRFS enclosed head assembly that is deployed down the borehole and an electronics control assembly consisting of a power supply and control electronics for the XRFS instrument. PC-based software provides the control, data readout, and quantitative calculations needed for interpretation of the XRFS spectra.

The excitation source is a silver anode X-ray tube (Comet NA, Stamford, CT) [see Appendix B]. The energy dispersive X-ray detector is a 7-mm^2 Si–PIN diode (Amptek, Inc., Bedford, MA) [see Appendix C]. This detector was chosen mainly because of the availability of a preamplifier compatible with the size restrictions. It has a good peak to background ratio and a 12-micron thick beryllium window for light element sensitivity. A digital pulse processor from the detector manufacturer (Amptek, Inc., Bedford, MA) converts the detector output to an energy spectrum [see Appendix C]. The energy calibration is linear and determined from the location of the iron characteristic emission and silver elastic scatter peaks. Because the borehole diameter cannot be controlled with precision, the collimation and beam definition geometry are optimized to allow for varying distance to the measurement volume at the borehole wall. The excitation beam is larger than the area viewed by the detector, making the signal less sensitive to the wall distance.

The performance requirement is to detect the elements magnesium through zirconium (atomic numbers 12 through 40 in the periodic table) and the elements cadmium through

lead (atomic numbers 48 through 82 in the periodic table).

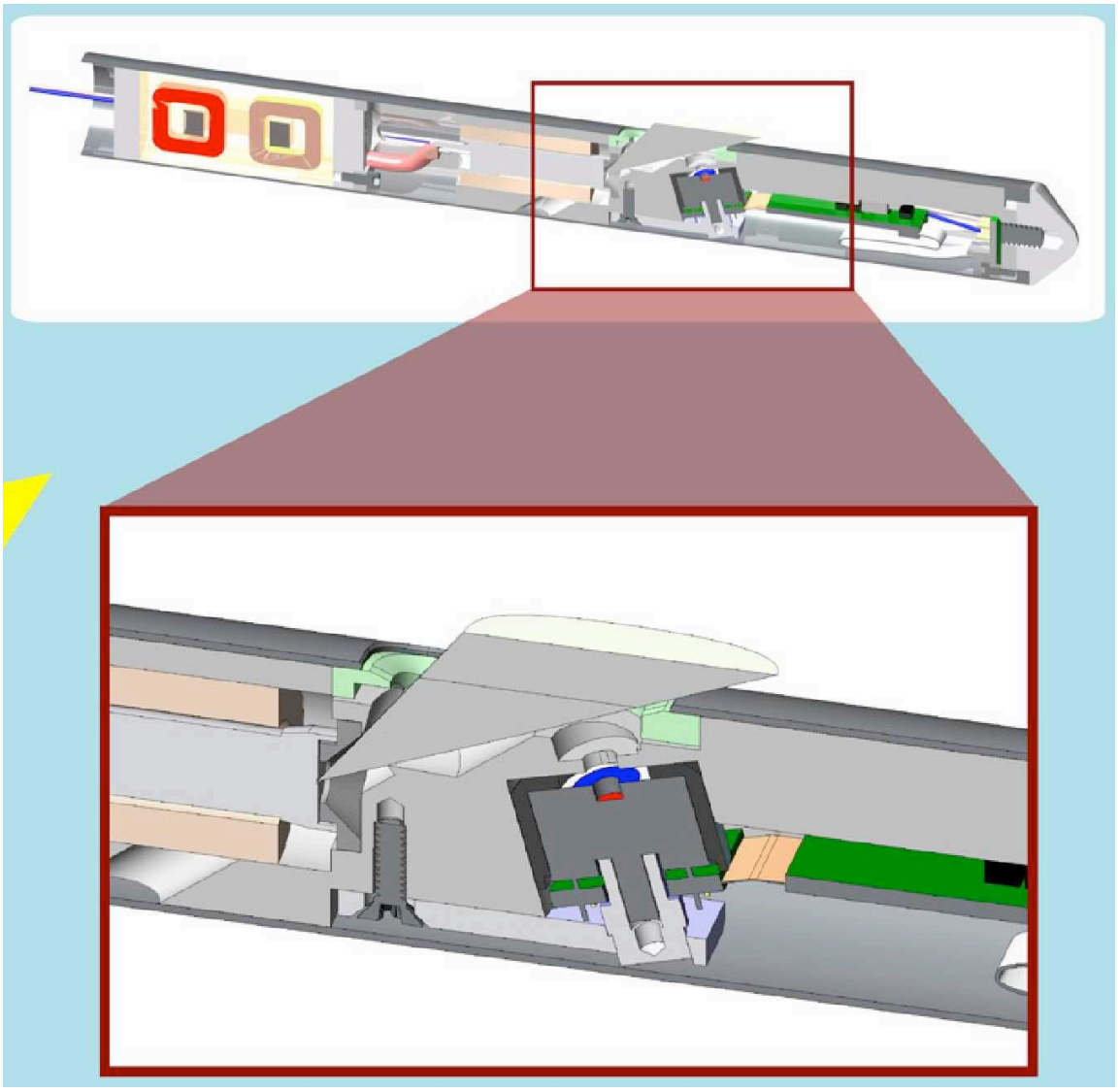

Figure 10. Engineering drawing of the final design of the downhole assembly. The enlarged area shows the X-ray tube and the detector.

Major hardware subsystems

The X-ray source is a miniature but otherwise conventional X-ray tube. It generates X-rays by bombarding a metal anode with high-energy electrons. The electrons are

produced in a hot filament and accelerated to high energy by a high voltage. The filament heater power controls the beam, or emission, current. The X-ray output is proportional to this current. The electron beam energy is controlled by the high voltage applied to the X-ray tube. This voltage determines the X-ray spectrum emitted by the tube and is one of the main parameters used to control the spectrometer. The X-ray tube has a very high vacuum inside and the X-rays exit via a thin window. Other parameters that influence the X-ray spectrum of the tube are the angles that the electron beam makes with the anode and the exit window, the material and thickness of the exit window, and, of course, the anode material.

The X-ray detector is based on a silicon diode that is reverse biased to provide a thick region of high-resistivity silicon with an electric field across it. The X-rays are absorbed in this region and produce electron–hole pairs in the silicon. The high electric field separates the electron–hole pairs and produces a pulse of charge at the electrodes of the diode. This pulse is amplified and its amplitude measured. Its amplitude is proportional to the energy of the absorbed X-ray. A digital pulse processor separates this pulse from the noise, determines its amplitude, digitizes the amplitude, and counts the pulses with matching amplitudes to collect a spectrum.

The silicon diode is taken to about –60ºC by Peletier cooling to reduce the noise and allow better resolution of the pulse amplitude. The energy resolution in the spectrum is limited by the electronic noise in the diode and is typically about 150 electron volts. The digital pulse processor is optimized for detecting and discriminating X-ray pulses from this diode from the background noise. The count rate (the maximum rate that X-rays can strike the detector) is limited to about 10,000 per second by the speed of the pulse processing. The count rate is determined by the material being measured and the strength of the X-ray source. The rate is typically adjusted by controlling the beam current in the X-ray tube, as described above.

Hardware physical units

The subsystems are packaged into three units: the **XRF Head** that goes down the borehole and makes contact with the material being measured, the **XRF Control Unit**, and the **XRF Interface Unit**.

The **X-ray Head** contains the X-ray tube and the silicon diode X-ray detector. It also has a filament isolation transformer for the X-ray tube to isolate the filament heating power from the high voltage. It contains a preamplifier for the detector to amplify the pulses before they travel over the connecting cable. The **X-ray Head** is as small as possible to go down the smallest pre-drilled hole and measure the composition of the regolith at various depths. The 15-ft. umbilical cable is permanently attached to the **Head Unit**; it connects the **Head** and **Control** units.

The **XRF Control Unit** contains all of the essential electronics to operate the X-ray tube and detector. It constitutes the electronics that would be required for a future spacecraft instrument. For the X-ray tube, there is the high voltage power supply (HVPS), the filament driver and regulator, isolation amplifiers to provide monitor signals for the voltage and current, and an over-current protection circuit. For the detector, the unit contains a power supply board and the digital pulse processor board.

The **XRF Interface Unit** contains the hardware necessary to adjust and monitor the X-ray tube voltage and current from the host computer, several interlock sensors for personnel safety, and the low voltage power supplies for the electronics. This unit contains all of the support equipment that is necessary to operate the spectrometer on the ground. There are several cables connecting the **XRF Interface** and **XRF Control** units. The **XRF Interface Unit** also connects to the host computer via USB, to the personnel safety outerlocks, and to the main power line.

The software described here interacts mainly with the data acquisition board used to control the X-ray tube high voltage supply and with the digital pulse processor board for the detector. These functions are described more fully beginning on page 26.

Typical Operation

A typical X-ray spectrum of terrestrial soil is shown in Figure 11. There are three significant features. First are the large peaks in the spectrum between 3 and about 15 keV. These peaks are from the elements in the sample and are the main features of interest. Second are the peaks between 15 and 20 keV. These are the characteristic peaks from the X-ray tube anode material (silver in this case) that have been scattered toward the detector by the sample. They can provide additional information but are not as straightforward to interpret. The third feature is the background under the peaks. The background is small in an XRF spectrum from a good spectrometer, allowing detection of even very small peaks from elements at very low concentrations (the minimum detection limit). However, it must be modeled and removed by the analysis algorithms to provide accurate measurements of the peak intensities.

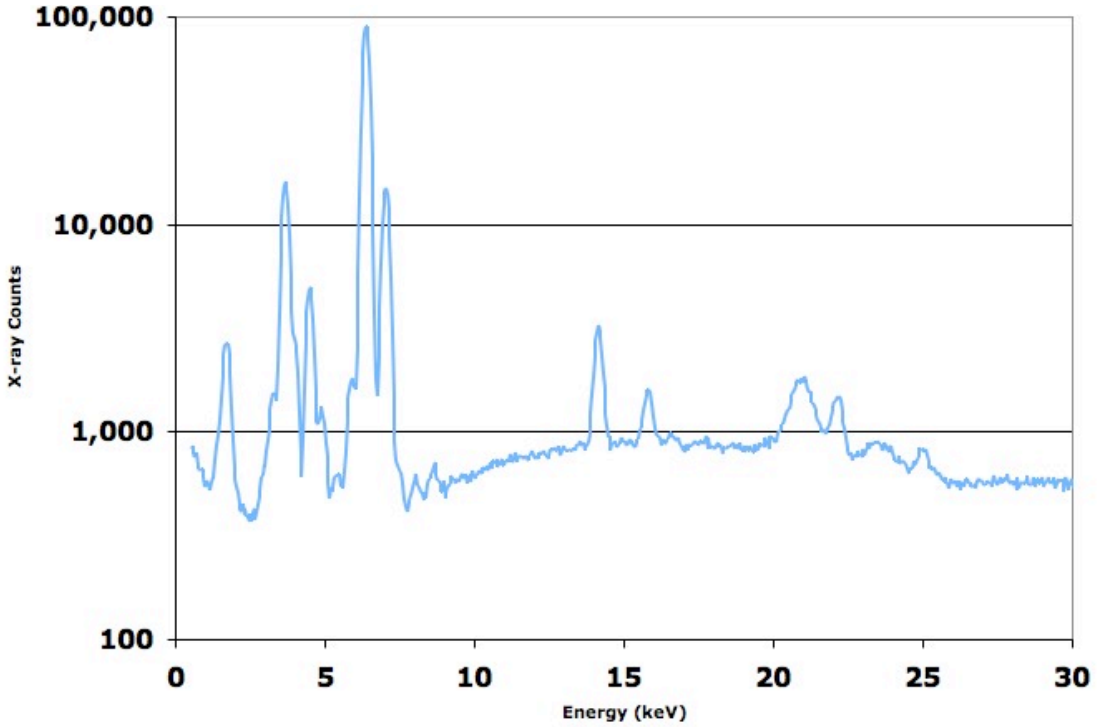

Figure 11. Fluorescence spectrum taken with the borehole XRFS. The soil sample was JSC1A Lunar Simulant.

Typical operation of the spectrometer by a user involves these steps. When power is turned on, the X-ray source is off (not producing X-rays) and the detector starts to cool down. The user places a specimen in front of the measurement window on the side of the XRF head (or places the head in a borehole).

The user then closes a radiation safety enclosure. When the safety enclosure is closed, a safety interlock switch closes, allowing the X-rays to be turned on. The voltage and current for the X-ray tube are set at this time, or previous settings are read in and used. The user chooses a data acquisition time, clears the spectrum in the digital pulse processor (DPP), and starts data acquisition. The spectrum is displayed as it is collected and the user will typically check the total count rate and make sure the spectrum looks correct (perhaps examining some regions more closely using zoom and pan). The user may be looking for particular elements, and will thus focus on the chosen elements. The

user will then stop the data acquisition, change any data acquisition parameters to optimize the spectrum, clear the spectrum, and collect the desired data.

The data are displayed as a function of the X-ray energy. To do this, the detector pulse height must be calibrated to match the X-ray energies. This is typically done using X-ray peaks from known elements. The calibration must be checked (typically daily) and may need to be repeated at irregular intervals.

Once data are collected, they can be stored in a file and/or analyzed further. Further analysis consists of modeling the background, finding any peaks in the spectrum and associating them with the corresponding elements, determining the net intensity of the peaks, and converting this net intensity into weight fractions of the elements. The background and a reconstruction of the spectrum using the extracted net intensities are displayed. This allows the user to quickly and visually evaluate the analysis of the spectrum. The element list and weight fraction of each element, together with estimated uncertainties, are also displayed.

The conversion from peak intensity to weight fraction is accomplished using a physical model of the interaction of X-rays with the material being analyzed. This model requires a complete description of the instrument to give accurate results. This description is more information than is typically changed by the user, such as fixed angles and distances within the components. It is also more information than the software needs to control the instrument. This information is read in from a parameter file and is usually not changed. It can be initially entered and changed via second-level dialogs that are invisible unless needed.

The user can also enter information about the material being analyzed and can change the instrument description information to be stored with the spectrum if desired. The data

acquisition parameters, such at X-ray tube voltage and current, are automatically stored with the spectrum.

The spectrum is stored in a file along with the information about the parameters under which it was acquired and enough of a description of the instrument to allow later analysis if necessary. The file format used is the standard format for energy-dispersive spectra adopted by the Microscopy Society of America and the European Microscopy Society.[1] Additional keywords were added to provide a complete description of the measurement conditions including instrument configuration (see Table 1).

[1] European Microscopy Society standard format, Version 1.0, see files emmff.doc and emmff.src, at http://www.amc.anl.gov/ANLSoftwareLibrary/02-MMSLib/XEDS/EMMFF/
There is a proposed format based on XML that is not yet standard. See file EMSA_MAS_V2_XML_MM8_2002.pdf

Hardware Description

XRF Interface Unit

Low voltage power supplies (COTS)

+/– 15 VDC for op-amps
+15 VDC, 1.5 amp for HV module
+5 VDC for interlocks and detector
Detector requires 0.5-A steady-state with 1-A startup surge lasting 30–60 sec.

DAQ and control board (COTS)

OnTrak ADR2000A

USB to serial adaptor (COTS)

Targus PA088

USB hub (COTS)

D-Link, Model DUB-H4, high-speed USB 2.0 4-port hub

Safety interlocks and control (APL-UW)

X-ray on/off

Purpose. Turns the X-ray tube on and off, including ramping filament up and down and safety disabling the high voltage module.

Background. This signal controls the main functions of the X-ray tube power supply system. It is disabled whenever one of the safety signals (see below) is absent. It will shut down and latch in the "off" condition whenever one of the safety signals disappears.

Operation. Logic circuit responds to a binary signal from the DAQ, tests all of the safety condition signals, and provides signals for HV disable, filament voltage ramp control, and status to the DAQ board.

Warning light and fail-safe

Purpose. Controls the warning light (115 V AC external lamp), turning it on and off with the X-rays. Provides a safety signal that indicates when the lamp is working.

Background. One of the federal safety requirements for X-ray systems is a warning light that turns on whenever the X-ray producing system is energized (defined as high voltage on). The light must be fail-safe in that the X-rays will not come on if the light bulb is burned out.

Operation. Solid-state relay to turn the power to the external socket on and off. A current detector (full-wave bridge rectifier in parallel with Zener diodes driving a 5-V DC relay) indicates that the external lamp is drawing current (i.e., connected and not burned out). The current detector does not provide a signal unless the lamp is energized, a delay must be provided that allows the lamp to be turned on, then X-rays must be turned off if the current detector does not indicate lamp operation. The delay is typically about 100 milliseconds.

Electrical interlock status

Purpose. An external signal provided by a user that indicates that all of the X-ray shielding is in place.

Background. Another federal safety requirement is that the enclosure that protects human operators from radiation exposure be interlocked to the high voltage supply. This interlock must disable the high voltage if the shielding is opened, to prevent accidental radiation exposure.

Operation. An external signal. It disables the high voltage power supply and prevent X-rays from being turned on (or shut them off if they are on). The signal is typically an external switch closure. It also disables the X-rays in case of a short to ground to prevent shorts from giving a false OK signal. A TTL or other logic signal is OK if +5 V or similar is available on the external connector to facilitate use with un-powered mechanical switches on a radiation enclosure.

Filament connector engaged

Purpose. To insure that the filament connector is inserted before the high voltage or X-rays are turned on.

Background. The commercial, miniature high voltage connectors used have only a contact for the negative high voltage, not for the positive return path (ground in this case). The ground return path is via the filament connector. If the high voltage is energized with the high voltage connector in place and the filament connector dangling, then a shock hazard condition can be produced.

Operation: A simple logic circuit that passes through the external filament connector via two extra pins.

Over-current signal

Purpose: See over-current cutoff under high voltage power supply board in the **XRF Control Unit** above. This signal is passed through to the DAQ and should remain after the X-rays are turned off until reset via the DAQ (usually by the X-rays off signal).

Background. This is just an interface to the over-current cutoff from the high voltage power supply board.

Operation. Logic circuit that is part of the X-ray on circuit.

Ground failure detect

Purpose. Insures that a safe return path for the high voltage exists and avoids potential shock hazards.

Background. If high voltage is applied to the X-ray tube and a connection between the X-ray tube anode and the return current path to the power supply ground fails, then a potential shock hazard exists. This circuit tests the ground return path by applying a voltage to the X-ray tube anode via a resistor, then testing to be sure that voltage is shorted to ground.

Operation. Applies a voltage through a pair of resistors, to the X-ray tube anode over the umbilical cable. One resistor is in the power supply and one is in the **XRF Head Unit** near the X-ray tube anode. This will produce a known voltage if the X-ray tube is properly grounded. If the umbilical cable lead is shorted, then the voltage will be zero. Provides a signal if the correct voltage is present, and disable the X-rays if not.

XRF Control Unit

High voltage power supply board

HV module (COTS)

Filament driver and regulator (APL-UW)

Purpose. Provides AC drive voltage for filament isolation transformer to heat filament. Regulates filament voltage to achieve emission current set point.

Background. The electron beam in an X-ray tube is generated from a hot filament at high negative voltage. The electrons emitted from the hot filament are accelerated by the high voltage and strike a metal anode at ground potential. The metal anode emits X-rays. The filament is heated by a current passing through the filament wire. Since the filament is at high negative potential, the heater current must be isolated by a filament transformer operating at 6 kHz. The electron beam current is regulated by the temperature of the filament, which is controlled by the filament heater current.

Operation. 6-kHz AC is generated by an oscillator, whose output voltage is controlled by a feedback loop. The output goes to a power audio amplifier chip to produce enough power and voltage to drive the filament transformer (which is located in the XRF Head). The feedback loop compares the current signal from the HV module to a set point and adjusts the filament heater voltage. The feedback has upper and lower limits (via a Zener diode), integration of the error signal (via a capacitor), and some linear gain for stability (via a resistor), all in the feedback leg of an op-amp. This regulator reverts to the "filament off" condition on power-up and wherever X-rays are turned off.

Isolation and amplification of HV monitor signal (APL-UW)

Purpose. To condition the signals from the HV module to achieve convenient gain and to protect the remainder of the circuits from spikes due to high voltage arcs.

Operation. Op-amps with diode and capacitor spike suppression at their inputs.

Over-current cutoff (APL-UW)

Purpose. To protect all of the hardware from a long-term overload condition.

Background. X-ray tubes sometimes develop arcs or plasma discharges. If they are brief, they usually clear themselves and are not a problem. But if they last for several seconds, they can overheat themselves or other components. This protection circuit serves as a backup to the software over-current protection. The HV module is also current-limited, but that only protects the module, not the X-ray tube.

Operation. Compares the emission current signal from the HV module to an on-board set point. If the emission current exceeds the set point for more than 5 sec, turn off the X-rays.

Detector power board (COTS)

AmpTek PC4-3

Detector pulse processor board (COTS)

AmpTek DP4. The detector system is completely isolated as well as electrically and magnetically shielded from the X-ray tube power supply, with one common ground point at the +5 volt power supply. The signals from the X-ray detector at the preamp output are pulses of about 10 microseconds duration and about 1 mV amplitude. Their amplitude must be measured to within a few percent to obtain a useable X-ray spectrum. Electronic noise is the major limitation and is minimized. Magnetic shielding is accomplished with co-netic foil.

Software Description

X-ray Tube Control (XTC)

Description

This module has two main purposes: to display and allow the user to change the parameters related to the X-ray tube, and to control the high-voltage power supply (HVPS) for the X-ray tube. The controls for this module are located on the main screen in the upper right corner of the interface (Figure 4).

The main parameters for the X-ray tube are the high voltage (kV) and the beam emission current (μA). Typical values are 35 kV and 2 μA. The user must also input a complete description of the X-ray tube for proper operation of the quantitative analysis software. These parameters are in a separate dialog that appears on request but is usually invisible (Figure 8).

The HVPS has a series of safety interlocks to prevent accidental exposure of personnel to high electrical voltages and X-ray radiation. The status of these interlocks is clearly visible to the user and turn red if any fail (Figure 12).

Control of the HVPS requires turning the X-ray on and off under user control, and responding to any changes in the interlock status by turning off the X-rays. The X-ray tube voltage and current settings are converted from the display units (kV and μA) to the DAC integer values and sent to the DAC using its commands. The actual values are read from the DAC and converted to the display units. When the X-rays are turned on, the X-ray tube must be ramped up to the operating conditions gradually (see ramp-up under functions).

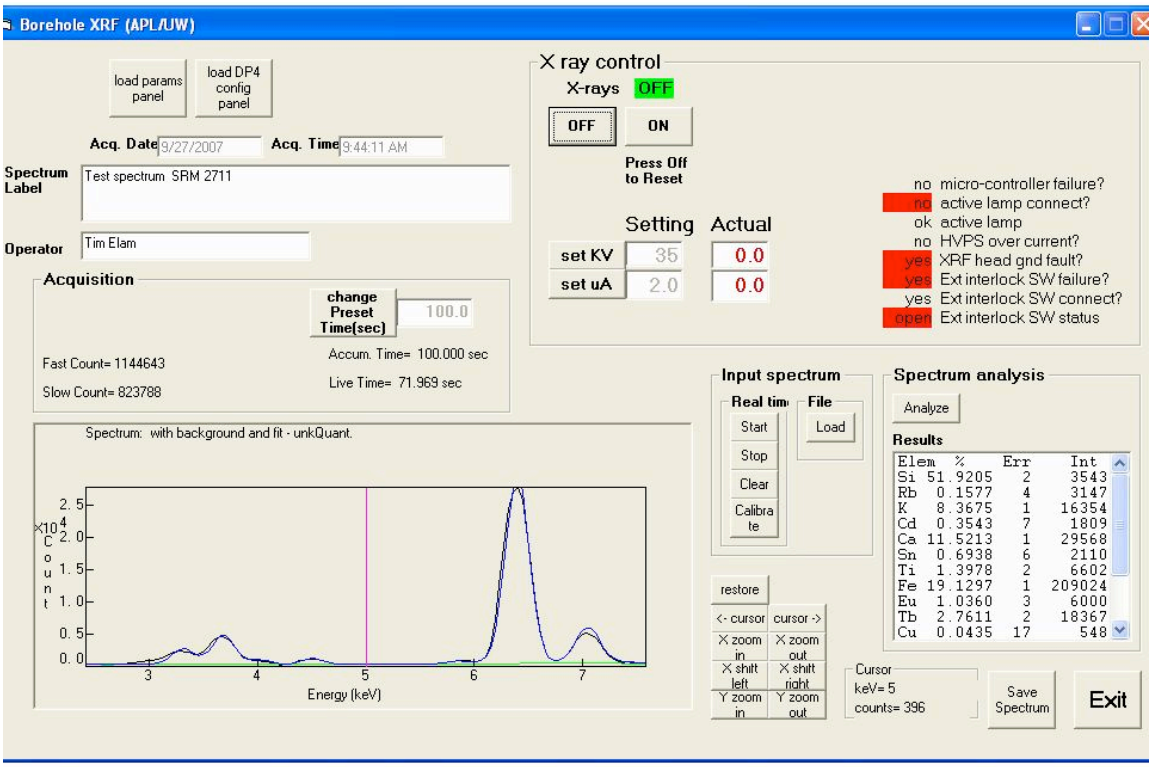

Figure 12. Borehole XRF interface indicating interlock failure

Functions

Set and display X-ray tube voltage (kV)

Set and display X-ray tube emission current (μA)

Check limits for X-ray tube parameters

Check and display status of safety interlocks

- X-ray on/off
- Warning light and fail-safe
- Electrical interlock
- Filament connector engaged
- Over-current signal
- Ground failure detect

Turn X-rays on and off

Ramp-up X-ray tube gradually to full operation

- Bring up kV to no more than 10 kV
- Bring up emission current to no more than 5 μA
- Raise kV and μA gradually together to specified values

Communicate with HVPS

- USB port or other communication parameters
- Commands to ADC and DAC
- ADC and DAC conversion constants

Set and display X-ray tube and instrument description

- X-ray tube type (side or end window)
- Anode material
- Be window thickness
- Electron incident angle
- Takeoff angle
- Aperture size and distance
- Filter material and thickness (if any)
- Path length from X-ray tube to specimen
- Angle that X-rays from tube strike specimen (incidence angle)

Detector Data Acquisition (DET)

Description

The X-ray detector acquires the spectrum; its associated electronics are commercial off-the-shelf. The manufacturer (Amptek, Inc., Bedford, MA) also supplies a library of communications and control routines that operate over a USB interface. The main function of the DET module is to drive these functions to acquire the spectrum (once the X-ray tube is operating and the user requests data be collected). As with the X-ray tube,

there are several data acquisition parameters that the user can change. Some of these appear on the main screen and some in a separate dialog (Figure 9).

The signal from the X-ray detector is analyzed by a digital pulse processor (DPP) that is specialized for energy-dispersive X-ray detector pulses. Many of the parameters for this DPP are software changeable but require specialized commands and some tuning procedures. The parameters are loaded at startup from a database.

One of the auxiliary functions of the detector data acquisition module is to check, set, and maintain the detector energy calibration (Figure 6). This calibration relates the channels in the spectrum (which are proportional to the pulse amplitude from the detector) to X-ray energy. The calibration is determined using the peaks of known elements, either in the spectrum from the material of interest if they are known or from a calibration sample. The energy calibration procedure consists of finding the location of the peaks, identifying the element associated with the peak, and including the peak positions and element energies in a calibration function. The function used is linear. The energy calibration will usually not change much day-to-day, so a stored calibration can be used. Any changes in the DPP tuning will change the calibration, so the DPP setup and calibration will force a re-calibration if any DPP parameters are changed.

Functions

Communicate with detector digital signal processor (COTS code)

Set and display data acquisition parameters

- Live time (seconds, calculated in DPP)
- Real time (seconds)
- Count rate (counts per second, display only)
- Dead time (%, display only)
- Total counts (display only)

- Chamber atmosphere (Earth ambient, Mars ambient, pure helium, vacuum)

Energy calibration (eV per spectrum channel)

- Set and display calibration constants
- Calculate energy vs. channel (linear or quadratic function)

Set and display detector parameters

- Aperture size and distance
- Path length from specimen to detector
- Energy resolution
- Window material and thickness
- Dead layer material and thickness
- Active layer material and thickness
- Angle that X-rays exit specimen toward detector (emergence angle)

Set and display digital pulse processor parameters

- (See manufacturer's manual, Appendix A)

Control digital pulse processor setup

Save and Load Parameters (PAR)

Description

This module handles all the parameters from other modules. The functions in this module are called at startup and shutdown, and by the other modules whenever any parameters are changed.

The module saves the parameters to a file and reads them from a file. The name and location of the parameter file are set and displayed by this module via a dialog (Figure 8). No other parameters are modified or displayed by this module. The file format is determined and controlled by this module.

Functions

Set and display parameter file name

Save all parameters to file

Load all parameters from file

Save and Load Spectrum (SSF)

Description

The spectrum is stored in a file that contains the spectrum data (counts per channel), the energy calibration that relates channels to X-ray energy, the parameters under which it was acquired, and the description of the instrument. Older files can be read in by the software and displayed and analyzed just as newly collected data are handled. All of the information necessary to display the spectrum and to allow later re-analysis if desired is stored in the spectrum file.

Functions

Set and display spectrum file name

Save data and all relevant parameters to file

Load data and all relevant parameters from file

File format

The file format is the standard format for energy-dispersive spectra adopted by the Microscopy Society of America and the European Microscopy Society.[2] Additional

[2] European Microscopy Society standard format, Version 1.0, see files emmff.doc and emmff.src, at http://www.amc.anl.gov/ANLSoftwareLibrary/02-MMSLib/XEDS/EMMFF/
There is a proposed format based on XML that is not yet standard. See file EMSA_MAS_V2_XML_MM8_2002.pdf

keywords (Table 1) were added to this format to allow inclusion of the instrument parameters used to analyze the spectrum.

Table 1. Keywords for XRFS spectrum output and parameter files added to the standard format for energy-dispersive spectra

Keyword	Description	Default value
kVsetting	X-ray tube kiloVolts Setting	20.00000000
uAsetting	X-ray tube microAmps Setting	5.00000000
kVscaleIn	kV Input Scale	-9.56999969
kVoffsetIn	kV Input Offset	0.00000000
uAscaleIn	uA Input Scale	24.50000000
uAoffsetIn	uA Input Offset	0.01000000
uAdividerR	uA Divider resistance (gigaOhm)	0.40500000
kVscaleOut	kV Output Scale	0.09380000
kVoffsetOut	kV Output Offset	-0.14000000
uAscaleOut	uA Output Scale	0.04100000
uAoffsetOut	uA Output Offset	0.10000000
RampInterval	Ramp Interval (sec)	1.00000000
kVdelta	kV Ramp Delta	1.00000000
uAdelta	uA Ramp Delta	5.00000000
kVstart	Minimum kV for Filament Start	10.00000000
kVlimit	kV Limit	40.00000000
uAlimit	uA Limit	25.00000000
anode_z	X-ray tube anode atomic number	47.00000000
kv	X-ray tube kiloVolts during acq.	20.21008301
tube_inc_angle	X-ray tube electron incident angle	90.00000000
tube_takeoff_angle	X-ray tube takeoff angle	51.11999893
tube_be_window	X-ray tube Be window (mm)	0.50000000
filter_z	Incident beam Filter atomic number	1.00000000
filter_thick	Incident beam Filter thickness (micron)	0.00000000
excit_angle	Incident beam Excitation angle (deg)	38.86999893
emerg_angle	Fluorescence Emergence angle (deg)	74.12000275
solid_angle	Solid Angle (sterdian)	0.00000850
path_type	Atmosphere Path type	2.00000000
inc_path_length	Incident path length (cm)	0.94000000
emerg_path_length	Emergence path length (cm)	1.97000003
window_type	Probe Window type	2.00000000
window_thick	Probe Window thickness (micron)	0.00000000
minimum_energy	Minimum analysis energy (eV)	1000.00000000

Spectrum Processing (SP)

Description

This module calls another written in C++ to handle all of the computations. The parameters needed by the physical model contained in the code are provided by the spectrum processing module to the C++ module. The results of the spectrum analysis are provided to the user in an on-screen list and to the spectrum display module. This includes the calculated background and peak fits, the list of elements found in the spectrum, and the weight fractions of each element with associated uncertainties (Figure 7). Net intensities of the associated peaks for each element are also displayed with the intensity error from the Poisson statistics of the spectrum in the list on the lower right corner of the interface.

The element identification and association of peaks with elements is fully automated but is not entirely reliable. The quantitative results can be copied to the clipboard and made available outside the program to prepare reports using the results of this instrument.

Functions

Background calculation and removal

Peak search

Element identification (associate peaks with elements)

Net peak intensity determination and calculated peak fits

Quantitative analysis (converting peak intensity to element weight percent)

Copy results to display

Spectrum Display (SD)

Functions

Plot spectrum vs. X-ray energy (Figure 5)

Overlay calculated background and peak fits

Display markers at characteristic element emission line energies

Scale, zoom, and pan

Instrument Performance Report

The purpose of this instrument is elemental analysis of regolith strata in a pre-drilled borehole to investigate the subsurface of Mars and possibly other bodies within the solar system. As such the primary performance criterion is the ability to quantify the elements present in a particular stratum in an acceptable time and with sufficient accuracy to obtain useful scientific information. For the purposes of this study, the detailed performance of the sensor was evaluated by measurements on the actual prototype. The main performance metric is the minimum detection limit (MDL). Improvements in the ability to detect an element imply improvements in the ability to quantify the amount present. Though there are some subtleties in this, the performance is dominated by the number of X-rays present in the spectrum, which is dominated by the source strength given the constraints on geometry and the available detectors for this instrument. The performance was evaluated by measuring the detection limits of target elements in a light element matrix.

The ability to accurately quantify a particular element is mainly limited by the precision with which its X-ray emissions can be measured. This is determined by the statistical variations in X-ray intensity due to the Poisson nature of their arrival times. In a given time interval the number of X-rays that are detected has an intrinsic variance (the square of the standard deviation) equal to the number of X-rays. This means that the relative standard deviation is one over the square root of the number. For a given geometry and sample composition, the number of X-rays detected from a particular element is proportional to the source strength and the measurement time.

Detecting an element depends on both the number of X-rays collected from that element and the background present even in the absence of that element. Because the background is also subject to the same variations, the MDL is usually taken as three times the

standard deviation of the background (converted to elemental concentration by an appropriate calibration coefficient). This is equal to three times the square root of the background counts in the spectrum. Both the desired signal and the background are proportional to the source strength. The background arises from scatter of the continuum from an X-ray tube and the detector peak-to-background ratio.

Materials and Methods

Standard Reference Materials

Standard Reference Materials (SRMs) numbered 2709, 2710, 2711, 97B and 2702 from the National Institute of Standards and Technology were used for the characterization tests. These SRMs are a set of selected soils with varying amounts of the basic soil elements and extra elements in the form of contaminants. Concentrations ranged from tens of percents for the basic soil components to below one part per million. This provided a wide range to evaluate the instrument.

Samples were received from the National Institute of Standards and Technology as fine powders. The samples were poured into specimen cups as received and presented to the instrument without further preparation. Mars environmental conditions were simulated on a laboratory bench-top using a glove bag. Eight millibar carbon dioxide partial pressure was chosen as representative of the Mars atmosphere. A gas mix of three volume percent carbon dioxide with helium making up the balance at Earth ambient pressure and gravity provided the same carbon dioxide density typical of Mars atmosphere. All measurements were made in this atmosphere.

Determining the Minimum Detection Limit (MDL)

A spectrum is collected of a known sample containing the element for which the MDL is desired. It is best to use a sample with a known element concentration less than 100 times the MDL. The largest peak from the element is found (usually K α or L α) and the background is determined by a linear fit to the spectrum on either side of the peak. To determine the total background counts the number of channels under the peak is multiplied by the average counts in the channels on either side of the peak. The gross peak counts are similarly determined by summing the counts in all channels under the peak. The net counts from the element are the gross counts in the peak minus the total background counts. Next the square root of the total background counts is multiplied by three, then multiplied by the ratio of the known element concentration to the net counts from the element. This yields the MDL in the same units as the known concentration. Note that this procedure assumes a linear relationship between net counts and concentration, which is a good assumption at low concentrations near the MDL. All MDLs given in this instrument performance report were calculated using this procedure.

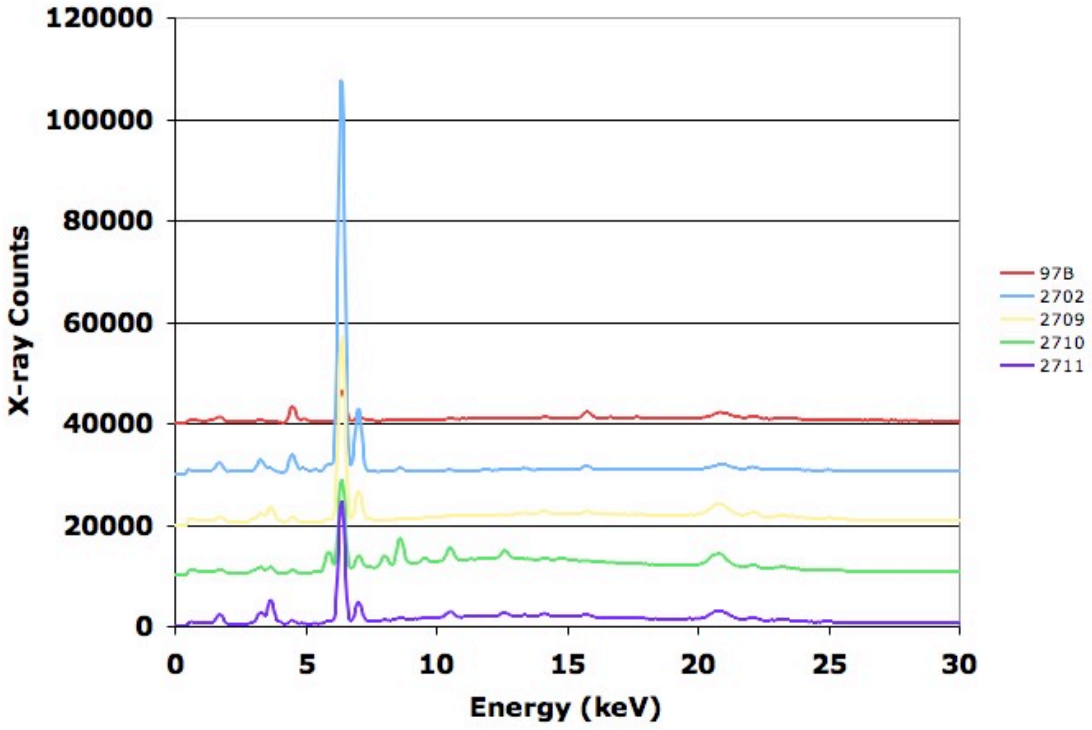

Figure 13. Raw spectra of five SRMs acquired with the borehole XRFS.

Test Plan Summary

- Determine the MDL for the elements Mg, Zr, Cd, and Pb
- Measure power consumption during spectrum collection
- Dry, water saturated, and frozen sample
- Variation with distance to probe (in case borehole diameter is not constant)
- Measurement stability vs. time
- Calibration linearity

Results

Figure 14 shows typical spectra from the borehole instrument. The specimen was a terrestrial soil, SRM 2709, measured in the Mars simulated atmosphere. The silver target X-ray tube was operated at 35 kV and 2 µA. No filters or other optics were used in the incident beam. The detector has an internal collimator to restrict the beam to the center of the diode. Data collection time was 1000 sec for the upper spectrum and 100 sec for the lower spectrum. Note that the majority of the information is still available even with the 100-sec data collection time. This short data collection will greatly facilitate the measurement of multiple strata in a borehole with vertical resolution of about 1 cm.

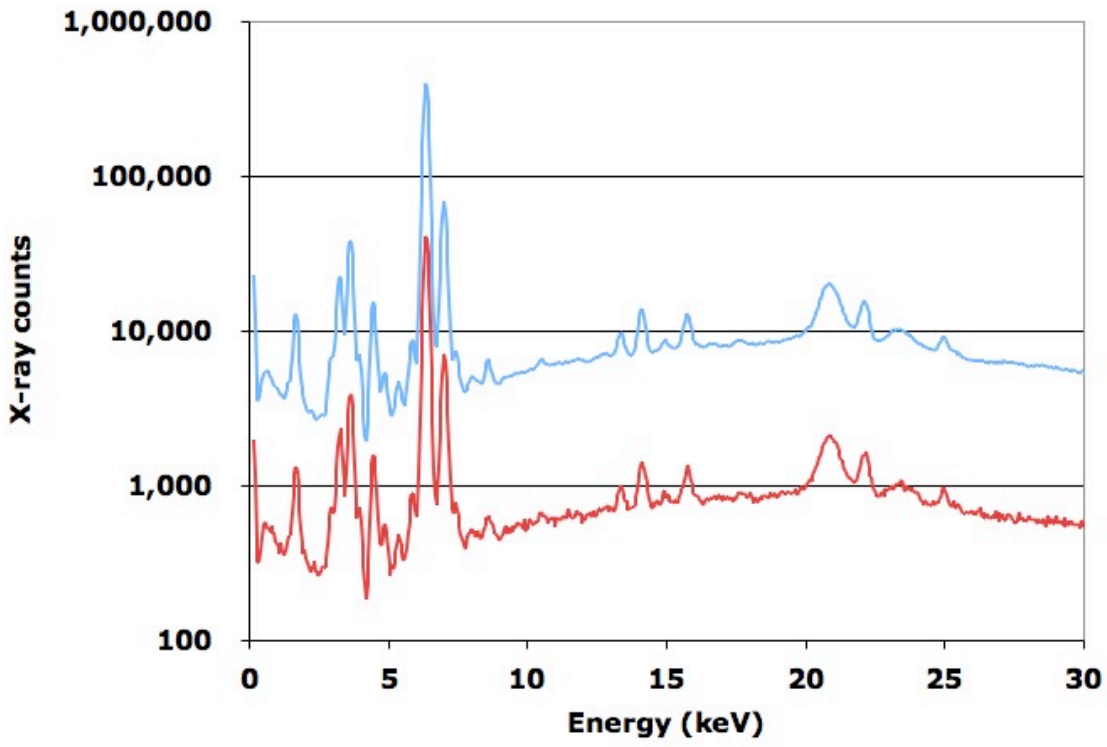

Figure 14. Spectra from borehole XRF spectrometer. Upper curve is 1000-sec data collection time, and lower curve is 100 sec.

As a comparison, the APXS (alpha proton X-ray spectrometer) spectra used on the Pathfinder and MER rovers have little usable data above the iron peaks at 6.4 keV (Figure 15). The spectrum acquisition times for both APXS curves were many hours. The scale is counts per second, so 1 corresponds to about 72,000 total counts.

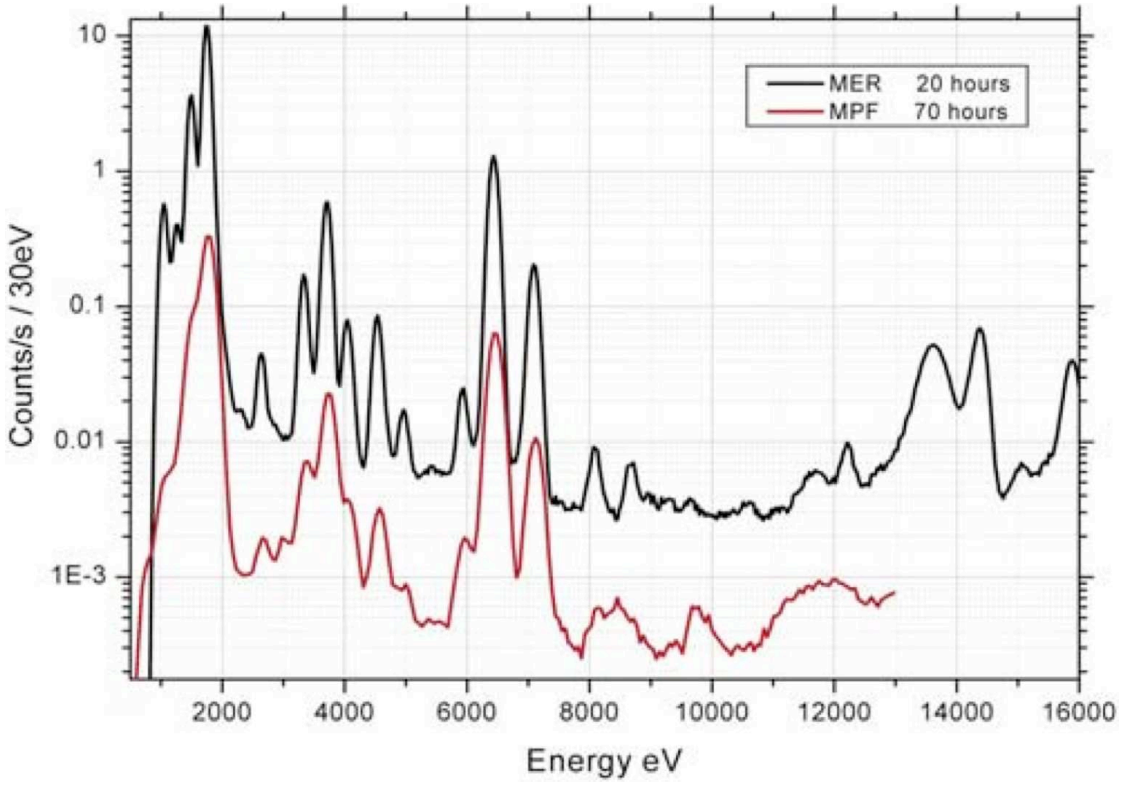

Figure 15. Spectra from the APXS instrument. Reproduced[3] with permission.

Detection limits for a number of elements in parts per million are presented in Table 2. They are computed using the three sigma method and assuming a linear relationship between net counts and the certified concentration. The background was linearly interpolated from the counts on either side of the peak. Detection limits for each SRM

[3] R. Reider, R. Gellert, J. Brückner, G. Klingelhölfer, G. Driebus, A. Yen, and S.W. Squyres, *J. Geophys. Res.,* **2003**, *108*, 8066–8078, DOI:10.1029/2003JE002150.

are given, along with the average values. SRM 2710 has rather high concentrations of many of the elements, so the linear concentration relationship may not hold. This causes the detection limits to be larger in this material. They were included in the averages since they have the effect of raising the detection limits, and including them avoids any bias toward lower values.

None of the SRMs contained Mg at a level that gave an unambiguous peak. A compound with magnesium as a major element was used to determine the magnesium detection limit. Talc, or magnesium silicate hydroxide, is a readily available magnesium compound (as baby powder, obtained from a local pharmacy) and was used for this purpose. Lowering the X-ray tube voltage to 20 kV decreased the magnesium detection limit from about 3% to the 1.4% value (Table 2). The ability to change the excitation conditions is another strong argument for using an X-ray tube.

Measured power consumption is given in Table 3 for the system components and the total. Ground support components including the safety interlocks and the USB computer interface are not included, as these functions are either not necessary in a spacecraft or are expected to be provided. The total power of 12 watts implies an energy requirement of 12 kJ per spectrum for a 1000-sec spectrum or 1200 J for a 100-sec spectrum. This is comparable to the APXS energy per spectrum, with larger power consumption but shorter collection times.

Table 2. Minimum detection limits for several elements

Element	2702	2709	2710	2711	97B	Average
Mg	ND	ND	ND	ND	ND	1.4%*
Ni	ND	8.9	2.0	ND	NP	5.5
Cu	8.2	4.2	16.2	8.9	NP	9.4
Zn	8.0	6.6	16.9	8.3	6.4	9.2
Pb	8.8	3.3	22.0	12.4	NP	11.6
Zr	NP	4.5	NP	4.1	4.8	4.5

ND = Not Detected NP = None Present

Table 3. Power consumption during data collection

Function	Voltage	Current	Power
HV Power Supply	+14.84 V	0.426 A	6.31 W
X-ray tube control	+14.92 V -14.92 V	0.150 A 0.149A	4.46 W
Detector	+4.99V	0.240A	1.20 W
Total			**11.97 W**

The effect on the measured spectrum from the presence of water is shown in Figure 16, where spectra from dry, water saturated, and frozen specimens of SRM 2702 are overlaid. There is almost no change in peak intensities, which is expected and indicates that good quantitative information can be obtained regardless of water content. Also, the presence of water will cause no significant degradation of detection limits. The region of the spectrum that has peaks from coherent (Rayleigh) and incoherent (Compon) scatter from the characteristic emission lines of the silver X-ray tube is shown in more detail in Figure 17. Note that the scatter is much larger in the saturated and frozen specimens. This increased scatter indicates presence of water and can be used to quantify the amount of water present.

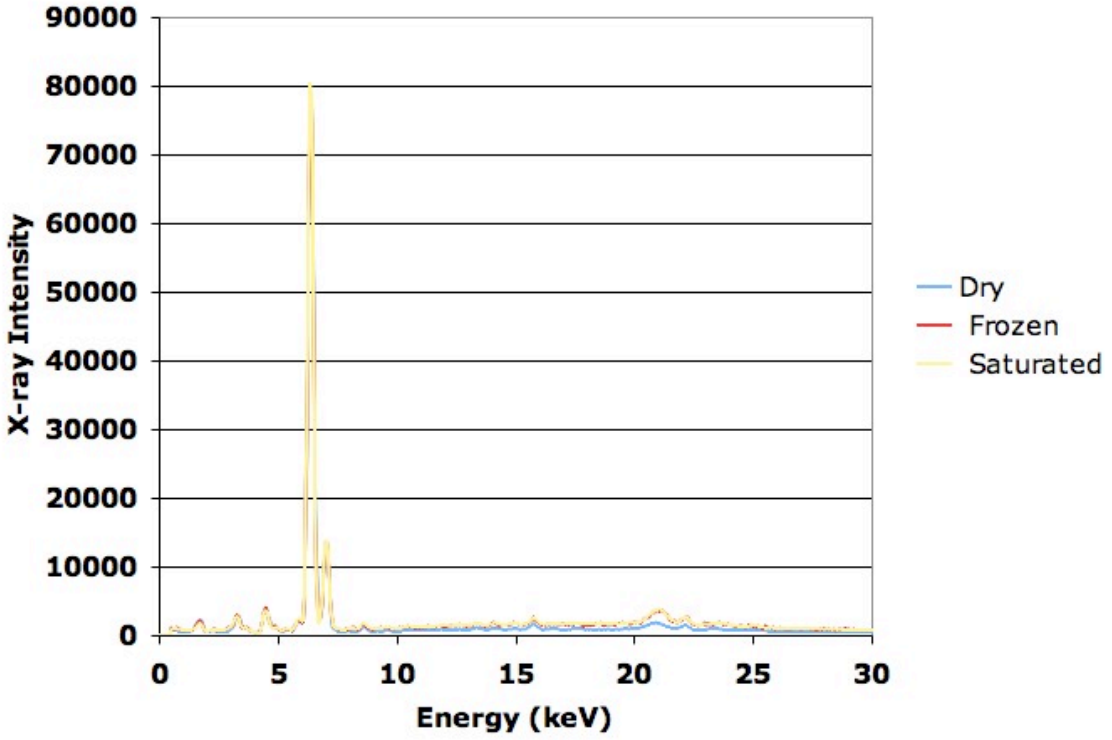

Figure 16. Spectra of dry, water saturated, and frozen samples of SRM 2702. (Frozen spectrum is 100 seconds to avoid thawing. It is multiplied by 10 for comparison.)

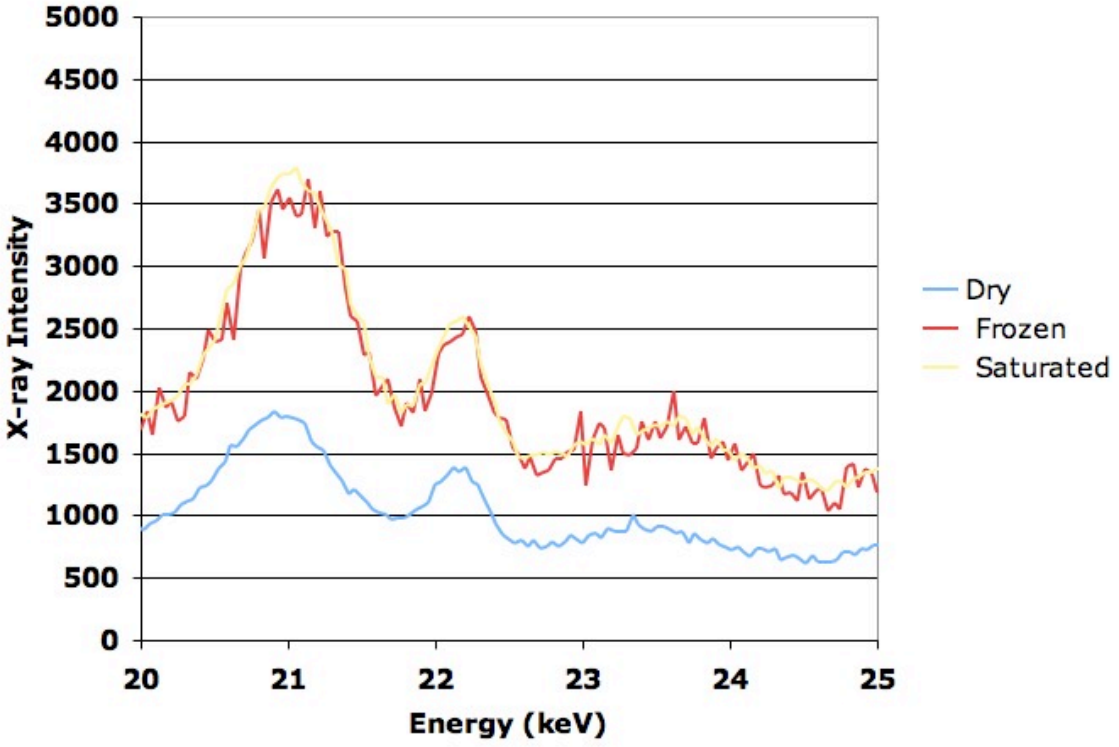

Figure 17. Spectra of dry, water saturated, and frozen samples of SRM 2702. (Frozen spectrum is 100 seconds to avoid thawing. It is multiplied by 10 for comparison.)

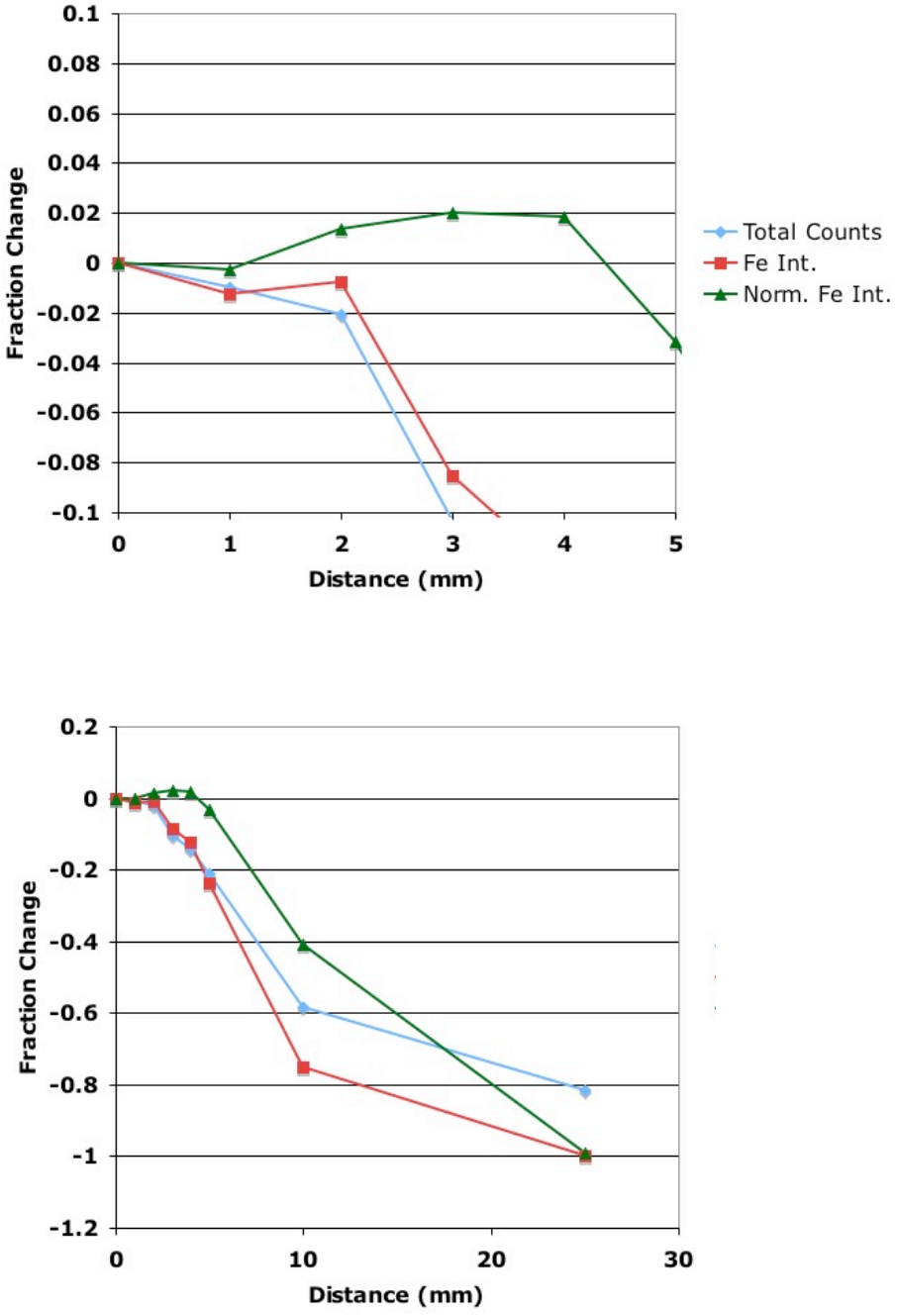

Figure 18. Variation in fractional change of total spectrum counts and iron intensity with distance to probe. Tests conducted with SRM 2711. Note different scales.

The results of varying the distance from the probe to the sample are given in Figure 18. The intensity in the iron peak and the total counts in the spectrum are plotted as a function of separation between the probe body and the sample surface. The plot on the left shows the behavior in the first few millimeters and the plot on the right shows all of the data taken for this test. Note that both of these measurements are stable to within 2% for as much as 2 mm of separation. In addition, the normalized iron intensity, which is the ratio of the iron peak to the total counts, is plotted as the green line. This quantity is stable out to almost 5 mm, indicating that accurate quantitation can be performed even at this distance. This is important since the diameter of the borehole may not be constant and thus the distance between the probe and the regolith being measured may vary. Because of the design, these expected variations will not affect the results of they are less than 2 mm and can be compensated for out to 5 mm. Beyond 10 mm the spectrum is no longer a reliable measurement of the sample.

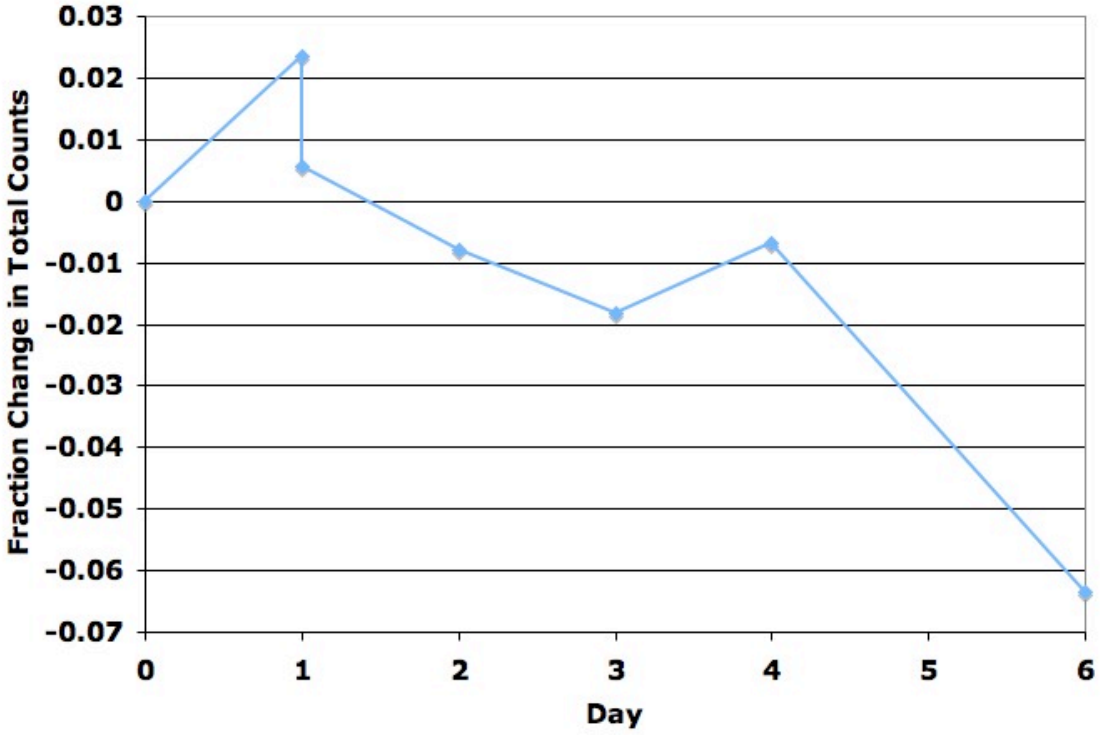

Figure 19. Variation in total spectrum counts over one week. (Point on Day 2 is after instrument was in continuous operation for 4 hr.)

Results of the measurement stability test are given in Figure 19. Stability is about 2% except for the final point. It is now known why this point is an outlier. The two points on day 1 were taken when the instrument was first powered on and after several hours of operation.

The calibration linearity was checked by plotting the composition measured by the instrument against the certified composition for all elements in all of the SRMs (below 10 weight percent) (Figure 20). Except for two outliers and several false positives (the points above the line near zero composition), the calibration is very good. The analysis algorithm used here is a "standardless" algorithm that relies entirely on the fundamental

parameters method to obtain the weight percent from the intensities in the spectrum. No standards were used in calculating these results. This is an advanced method that is not as good as careful use of type-specific standards, but was incorporated into the probe software because standards that are similar to the planetary regolith may not be available, especially if the subsurface regolith composition is unknown. Further work on the fundamental parameters analysis algorithm should improve the calibration performance. For the best results, appropriate standards with certified compositions can be used with an empirical correction algorithm.

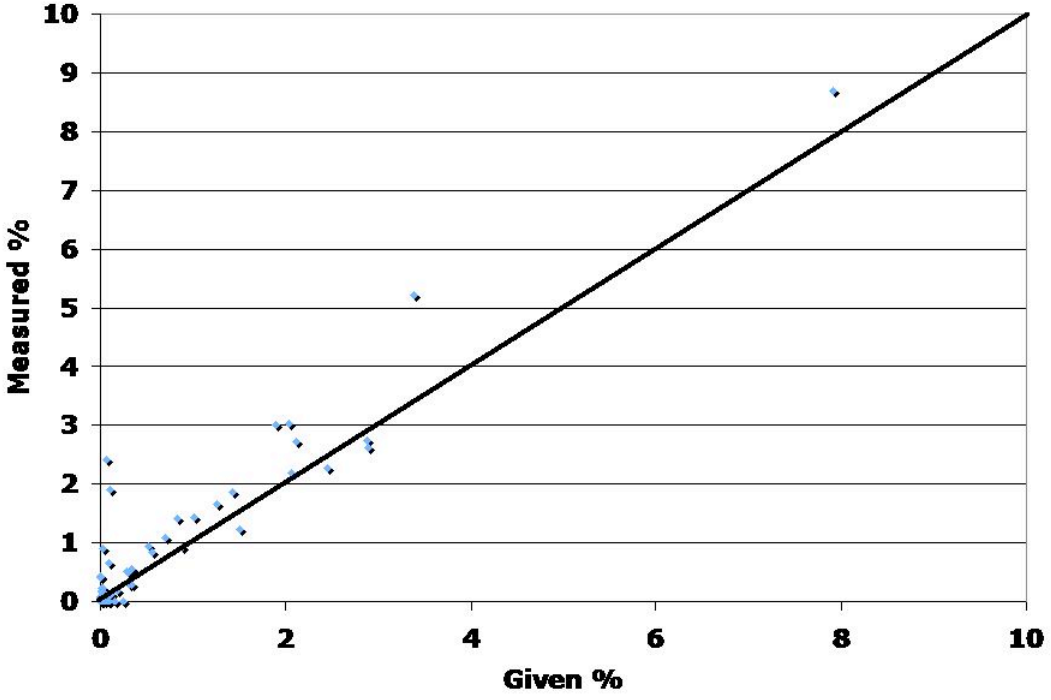

Figure 20. Measured vs. given composition for a wide range of elements in all five standard reference materials.

Conclusions

A borehole X-ray fluorescence spectrometer (XRFS) has been successfully constructed and tested. Miniaturization has been performed to a diameter of 27.1 mm and components can be configured in a variety of XRFS instrument designs. Modifications can be easily incorporated, such as an SDD detector, the use of a different target X-ray tube, or use of radioactive sources for excitation. Performance is very good, with detection limits of about 10 ppm for many elements and detection of light elements down to magnesium at 1.4%. Power consumption is 12 watts during data collection and the total energy per spectrum is comparable to previous planetary inorganic analysis instruments. Adequate data can be collected in 100 sec, facilitating investigation of strata with vertical resolution of about 1 cm in a reasonable time.

Appendices

All appendices are available on the CD-R that accompanies this report.

Appendix A. Digital Pulse Processor: User's Guide and Operating Instructions

Appendix B. X-ray Tube Product Documentation

Appendix C. Detector specification sheet

Appendix D. Borehole XRFS wiring diagrams

Appendix E. Borehole XRFS safety interlock/control board schematic

Appendix F. Borehole XRFS HVPS power and control board schematic

Appendix G. Borehole XRFS head unit and umbilical cable schematics

Appendix H. Borehole XRFS safety interlock/control board layout

Appendix I. Borehole XRFS HVPS power and control board layout

Appendix J. Bill of materials for safety interlock control

Appendix K. Bill of materials for HVPS power and control board

Appendix L. Borehole XRFS detector interface board schematic

Appendix M. Borehole XRFS detector interface board layout

Appendix N. Borehole XRFS safety controller software program by Peter Sabin

REPORT DOCUMENTATION PAGE

Form Approved
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The X-ray fluorescence spectrometer (XRFS) is designed to be deployed down a pre-drilled hole for exploration and elemental analysis of subsurface planetary regolith. The spectrometer excites atoms in the regolith and causes them to emit their characteristic X-rays. These characteristic X-rays produce peaks in the X-ray spectrum. By measuring the energy of the X-rays, elements are identified. By measuring the intensity of the peaks, the amount of each element can be determined. A software package operates the spectrometer, acquires the data, and analyzes the spectrum to provide elements and their weight fractions. It also provides a user interface to control the measurements and display the results.

The spectrometer consists of two main subsystems packaged in three physical units. The main subsystems are the X-ray source and the energy-dispersive X-ray detector. The source provides the X-rays to excite the specimen of regolith being investigated. The energy-dispersive X-ray detector detects the emitted X-rays, determines their energy (the energy-dispersive function), and counts the X-rays at each energy. Together these two subsystems measure the X-ray spectrum of the specimen.

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User's Guide and Operating Instructions

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1 DP4 Design and Operation 3
1.1 Major Function Blocks 3
1.2 DP4 Input 4
1.3 Pulse Shaping and Selection 5
1.4 DP4 Interface 10
2 DP4 Specifications 11
2.1 Connections 11
Controls and Adjustments 15
3 Quick Start Instructions 18
3.1 Set-Up Instructions 19
3.2 Configuring the DP4 21
3.3 Taking data 21
4 Control and Display Demonstration Software 23
5 Programmer's Guide 26
5.1 RS232 Serial Interface 26
5.2 USB Interface 26
6 Use of the DP4 with Amptek's XR100 Detectors 35
6.1 Users with a Standard XR100 and PX2 35
6.2 Users with a Standard XR100 without a PX2 38
6.3 Users with a DP4, PC4-3, and PA-210 Peamplifier 39
6.4 Analog Prefilter Circuit Description 41
6.5 Procedures for Common Changes 43
7 Dead Time in the Amptek DP4 46
7.1 Fast Channel 46
7.2 Slow Channel 47

7.3 Acquisition Time....48
7.4 Timing Summary....49
8 Trouble-Shooting Guide....49
9 Index....49

1 DP4 DESIGN AND OPERATION

1.1 MAJOR FUNCTION BLOCKS

The DP4 is a component in the complete signal processing chain of a nuclear instrumentation system, as shown in Figure 1. The input to the DP4 is the preamplifier output. The DP4 digitizes the preamplifier output, applies real-time digital processing to the signal, detects the peak amplitude (digitally), and bins this value in its histogramming memory, generating an energy spectrum. The spectrum is then transmitted over the DP4's serial interface to the user's computer.

The Amptek DP4 has 6 main function blocks to implement these functions: (1) an analog prefilter, (2) an ADC, (3) a digital pulse shaper, (4) pulse selection logic, (5) histogram logic, and (6) interfacing hardware (which includes a microcontroller) and software. These six functions will be discussed below. Clearly, the DP4 must be used with other components, including (at a minimum) a detector and preamplifier, a computer with a serial interface and software to communicate, and a power supply.

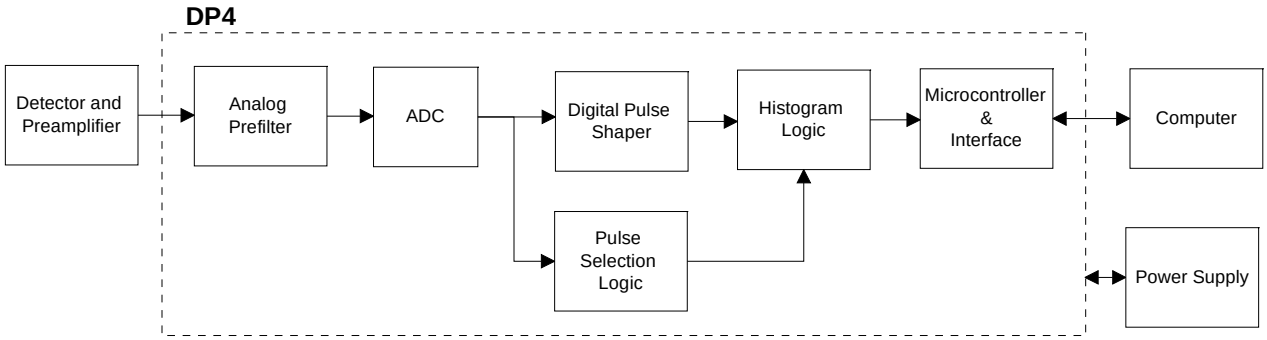


Figure 1. Block diagram of the DP4 in a complete system.

It is important to recognize that the DP4 is designed for OEM use as part of a complete instrument. It can also be tailored for laboratory use, but it is not intended as a stand-alone module for general purpose use. Amptek's PX4 is a general purpose laboratory module which includes the functionality of the DP4 and much more, such as power supplies. Amptek strongly recommends the PX4 for non-OEM users.

The DP4 interface and control hardware are designed with considerable flexibility so the OEM user can tailor it to a specific application. Amptek supplies software with the DP4 that includes two fully functional demonstration programs. One program runs on the embedded microcontroller and interfaces between the pulse shaping/histogram functions and a PC. The other program runs on a PC and interfaces between the DP4 and the user. Both of these are intended as demonstration programs, which the user will tailor. The DP4 also includes an FPGA. The FPGA logic, the "FPGA Configuration Bitstream", is copyrighted by Amptek, Inc. and may not be copied, modified, or used without the express, written approval of Amptek, Inc.

Analog Prefilter: The input to the DP4 is the output of a charge sensitive preamplifier. The analog prefilter circuit prepares this signal for accurate digitization. The main functions of this circuit are (1) applying appropriate gain, offset, and inversion (if necessary) to utilize the dynamic range of the ADC, and (2) carrying out some filtering and pulse shaping functions to optimize the digitization.

ADC: The ADC digitizes the output of the analog prefilter at a 20 MHz rate. This stream of digitized values is sent, in real time, into the digital pulse shaper.

Digital Pulse Shaper: The ADC output is processed continuously using a pipeline architecture to generate a real time shaped pulse. This carries out pulse shaping as in any other shaping amplifier. The shaped pulse is a purely digital entity. Its output can be routed to a DAC, for diagnostic purposes, but this is not necessary. The peak value of the digital shaped pulse is determined by a peak detect circuit in the pulse shaper. The peak value for each pulse, a single digital quantity, is the primary output of the pulse shaper.

Pulse Selection Logic: The pulse selection logic rejects pulses for which an accurate measurement cannot be made. It includes pile-up rejection and risetime discrimination. These are discussed in more detail below.

Histogram Memory: The histogram memory operates as in a traditional MCA. When a pulse occurs with a particular peak value, a counter in a corresponding memory location is incremented. The result is a histogram, an array containing, in each cell, the number of events with the corresponding peak value. This is the energy spectrum and is the primary output of the DP4. The DP4 uses 3 bytes per channel, which allows up to 16.7M counts per channel.

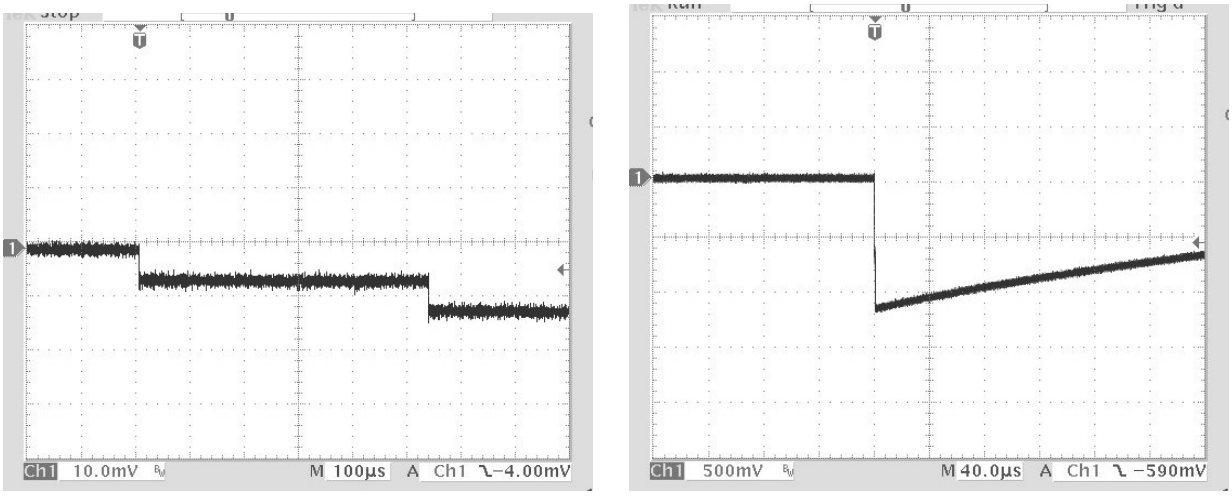
Interface: The DP4 includes hardware and software to interface between these various functions and the user's computer. A primary function of the interface is to transmit the spectrum to the user. The interface also controls data acquisition, by starting and stopping the processing and by clearing the histogram memory. It also controls certain aspects of the analog and digital shaping, for example setting the analog gain or the pulse peaking time.

The interface includes a microcontroller and serial interface hardware. Both RS232 and USB interfaces are currently implemented and described in this manual. The interface also contains an I^2C interface and several unallocated microcontroller pins that are available to the user. The interface includes two distinct software packages, embedded software which runs on the microcontroller on the DP4 and acquisition and control software that runs on the attached personal computer. The DP4 is shipped with a demonstration version of the acquisition and control software package (Visual Basic 5 source code is provided.) Source code for the embedded software (8051 assembly language) is also available – contact Amptek for more information.

1.2 DP4 INPUT

The DP4 was designed to process signals coming directly from a charge sensitive preamplifier used with a solid-state radiation detector. These signals typically have (1) a small amplitude, in the range of a few mV, (2) a fast rise (tens of nsec to μsec), and (3) following the signal, either a slow decay (of order msec) or no decay. A charge sensitive preamplifier integrates the current into its input, so over time the output drifts towards the rail. One of two methods is usually used to restore the output.

Some preamplifiers use a pulsed reset to periodically restore the input charge. In such preamps, there is no tail after the signal. A radiation interaction generates a voltage step, then the output is constant until the next step, as illustrated in Figure 2(a). Eventually, the output will drift near the supply rail and is then reset to its initial value, leading to a very large and fast reset signal. The DP4 is configured from the factory for use with such reset-type preamplifiers. The reset results in a large, negative going pulse into the ADC, which disrupts the signal processing. The preamplifier output can take a significant time to fully recover from a reset. Pulses received during reset recovery will have a distorted amplitude and degrade the spectrum. Therefore the DP4 includes hardware to lock out data acquisition during reset.



(a) (b)

Figure 2. Oscilloscope traces showing typical preamplifier outputs, for reset (a) and continuous (b) preamplifiers. The DP4 is shipped from the factory configured for the reset inputs, such as those on the left.

Some preamplifiers use a continuous feedback, the simplest of which is a resistor in parallel with the feedback capacitor. After the voltage step due to each signal interaction, the output slowly drifts back to its quiescent value, with the time constant of the feedback, as illustrated in Figure 2(b). This time constant is long, 500 μsec in this case, so that the charge in the signal can be accurately integrated. The DP4 hardware may be configured for use with most continuous feedback preamplifiers. This is discussed in Section 0

1.3 PULSE SHAPING AND SELECTION

1.3.1 Pulse Shaping

The DP4 implements trapezoidal pulse shaping, with a typical output pulse shape shown in Figure 3. This shape was chosen because it provides a near optimum signal to noise ratio for many detectors, including Amptek's XR100 detectors under normal operating conditions. The user can adjust the rise/fall time (the rise and fall must be equal) and the duration of the flat top. These values can be set to a large number of discrete values, shown in Table 1.

A semi-gaussian amplifier with shaping time τ has a peaking time of 2.2τ and is comparable in performance with the trapezoidal shape of the same peaking time. So, if the DP4's digital shaper were to be set to the equivalent of an analog amplifier with a 12 μs shaping time constant it would be set to roughly 2.2*12 = 26.4 μs peaking time.

The electronic noise of a detector will generally have a minimum at some peaking time, the "noise corner." At peaking times shorter or longer than this, there is more noise and hence degraded resolution. If this peaking time is long relative to the rate of incoming counts, then pulse pile-up will occur. In general, a detector should be operated at a peaking time at the noise corner, or below the noise corner as necessary to accommodate higher count rates.

If the risetime from the preamp is long compared with this peaking time, then the output pulses will be distorted by ballistic deficit. In this case, the trapezoidal flat top can be extended to improve the spectrum. The specific optimum timing characteristics will vary from one type of detector to the next and on the details of a particular application, e.g. the incoming count rate. The user is encouraged to test the variation of performance on these characteristics.

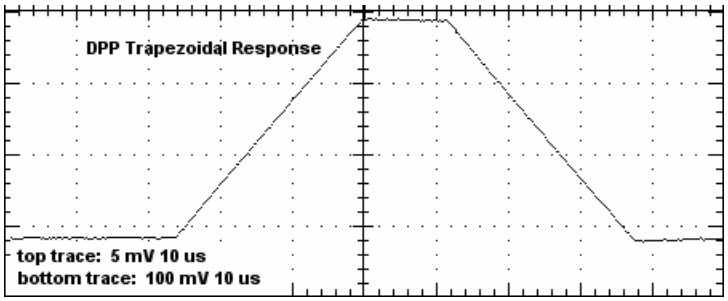


Figure 3. Pulse shape produced by the DP4.

Peaking Time (uS)	Flat Top (uS)	Decimation	'Rise' register	Flat Top register	Decimation register
0.8	0.2...3.2	1	1	0…15	0
1.6	0.2...3.2	1	2	0…15	0
2.4	0.2...3.2	1	3	0…15	0
3.2	0.2...3.2	1	4	0…15	0
4.0	0.2...3.2	1	5	0…15	0
4.8	0.2...3.2	1	6	0…15	0
5.6	0.2...3.2	1	7	0…15	0
6.4	0.2...3.2	1	8	0…15	0
8.0	0.4...6.4	2	5	0…15	1
9.6	0.4...6.4	2	6	0…15	1
11.2	0.4...6.4	2	7	0…15	1
12.8	0.4...6.4	2	8	0…15	1
16.0	0.8...12.8	4	5	0…15	2
19.2	0.8...12.8	4	6	0…15	2
22.4	0.8...12.8	4	7	0…15	2
25.6	0.8...12.8	4	8	0…15	2
32.0	1.6...25.6	8	5	0…15	3
38.4	1.6...25.6	8	6	0…15	3
44.8	1.6...25.6	8	7	0…15	3
51.2	1.6...25.6	8	8	0…15	3
64.0	3.2...51.2	16	5	0…15	4
76.8	3.2...51.2	16	6	0…15	4
89.6	3.2...51.2	16	7	0…15	4
102.4	3.2...51.2	16	8	0…15	4

Table 1. Table of allowed rise/fall times (peaking times) and flat top times.

The pulse shaping of the DP4 is illustrated in Figure 4. The top trace shows the input to the DP4, which is the output from a reset-type charge sensitive preamplifier. This is processed by the analog prefilter (see Figure 1), producing the prefilter output shown at the bottom. This is digitized and then processed digitally, producing the DP4's shaped output, also shown at the bottom.

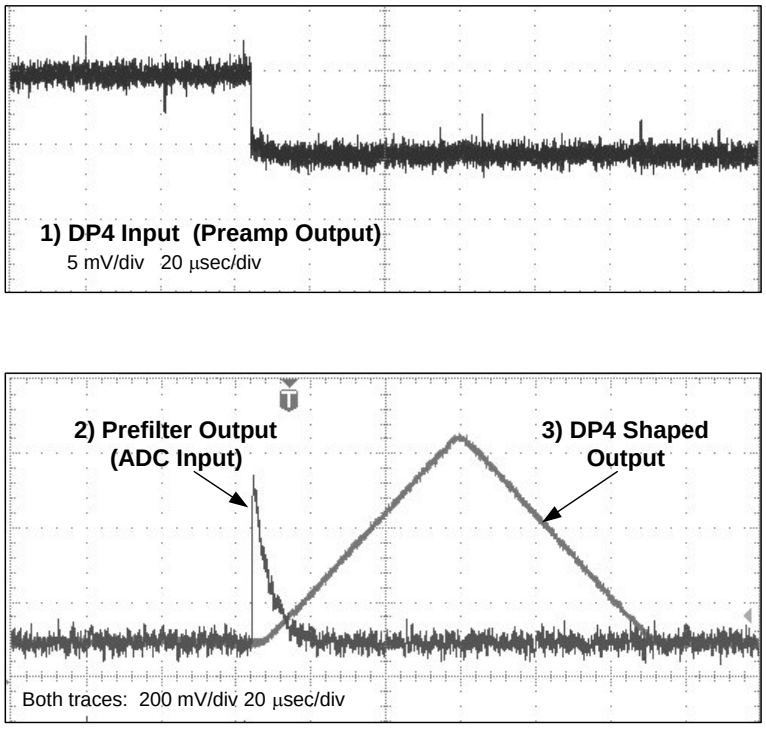


Figure 4. Oscilloscope trace illustrating the normal operation of a DP4.

1.3.2 Baseline Restoration (BLR)

The "baseline" of a digital processor has some significant differences from traditional analog shaping amplifiers. Traditional amplifiers generally include some form of baseline restoration, DC feedback, to prevent drift at high count rates. Because the DP4's transfer function has a finite impulse response, after a pulse has passed through the processing pipeline it has no impact on the output. This is fundamentally different from an analog differentiator and results in vastly enhanced baseline stability at high count rates. However, unlike analog shapers the DP4 has to establish a DC baseline, at all count rates. There are two options available in the DP4 to establish the DC baseline: "auto-baseline", which involves measuring the input offset, and baseline restoration, which uses closed loop, quasi-DC feedback.

1.3.2.1 Auto-Baseline

The 'Auto-Baseline' function does not correct baseline variations resulting from count-rate changes or other detector effects; rather, it corrects for drift in the DP4's analog section, due mostly to temperature changes. It is intended to be used with reset-style preamps that do not otherwise require BLR (i.e. the Amptek XR100CR). When the DP4 detects that reset has occurred, it temporarily disconnects the detector from the DP4 front-end electronics and averages the voltage offset produced by the front end. The detector is reconnected and the measured offset is used to correct the digital baseline. This doesn't affect throughput since the processing is suspended anyway during reset to allow the preamp signal to settle.

1.3.2.2 BLR

The DP4 also has an asymmetric baseline restorer, which can be used when baseline shifts due to count-rate changes, power supply drift, or if other detector effects need to be nulled. It works as follows:

a. All digital samples below the existing baseline are integrated. When the sum reaches a preset value (the "BLR Correction Threshold"), an upward correction (the "Baseline Up Correction") is added to the baseline.

b. Countering this occasional upward correction is a periodic downward correction (the "Baseline Down Correction.)

As the magnitude of these corrections is typically much less than one channel, the periodic downward correction and occasional upward correction should not adversely affect resolution. Each of the corrections has four settings (very slow, slow, medium and fast) and the correction threshold also has four settings (very fast, fast, normal and slow.) It should be noted that the relative size of these corrections is dependent on peaking time; thus a setting that works well at a particular peaking time may not necessarily be ideal for a different peaking time.

BLR and Auto-Baseline should not be used at the same time.

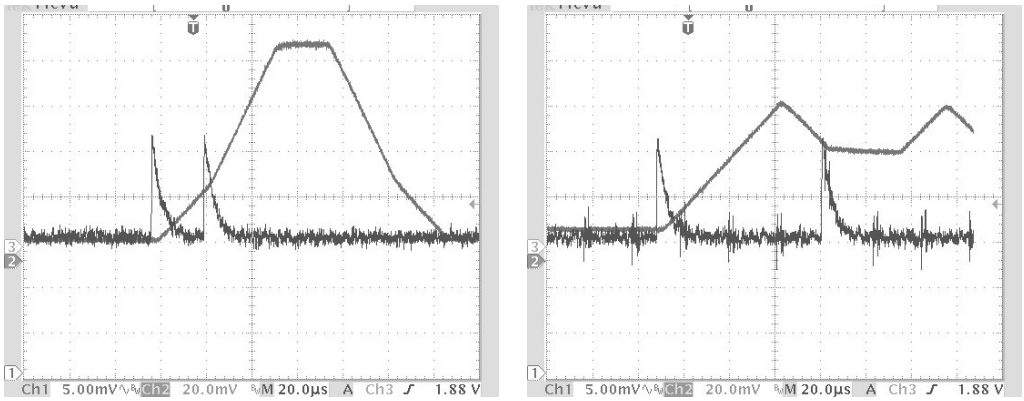
1.3.3 Pulse Selection

1.3.3.1 Pile-Up Rejection

The goal of the pile-up reject (PUR) logic is to determine if two interactions occurred so close together in time that they appear as a single output pulse with a distorted amplitude. The DP4 PUR uses a "fast-slow" system, in which the pulses are processed by a fast shaping channel in parallel with the slower main channel (both channels are purely digital). Though similar in principle to the techniques of an analog shaper, the pile-up reject circuitry and the dead time of the DP4 differ in significant ways, resulting in much better performance at high count rates. First, the symmetry of the shaped pulse permits the dead time and pile-up interval to be much shorter. Second, there is no dead time associated with peak acquisition and digitization, only that due to the pulse shaping. [Setting 0 = off].

Figure 5 illustrates the operation of the DP4 for pulses that occur close in time. Figure 5 (a) shows two events that are separated by less than the rise time of the shaped signal, while Figure 5 (b) shows two pulses that are separated by slightly longer than the rise time. In (a), the output is the sum of the two signals (note that the signal amplitude is larger than the individual events in (b)) and the events are said to be piled up. However, note that the analog prefilter outputs in (a) are separate. For a nearly triangular shape, pile-up only occurs if the two events are separated by less than the peaking time, in which case a single peak is observed for the two events. The interval used by the DP4 for both dead time and pile-up rejection is the

sum of risetime, plus about 20% of the risetime to account for jitter, and the flat-top duration. If two events occur within this interval and pile-up rejection is disabled, then only the single, piled-up value is in the spectrum. If pile-up rejection is enabled and two events are separated by more than the fast channel pulse pair resolution (600 nsec) and less than this interval, both are rejected. Events that exceed a threshold in the fast channel trigger the pile-up reject logic.



(a) (b)

Figure 5. Oscilloscope traces illustrating the dead time and pile-up reject performance of the DP4

1.3.3.2 Risetime Discrimination

In some types of detectors, pulses with a slow risetime have a charge amplitude deficit. For example, in many diodes there is an undepleted region with a weak electric field. A radiation interaction in this region will generate a signal current, but the charge motion is slow through the undepleted region. This leads to a slow rising edge on the pulse and since charges are trapped, a small pulse. Interactions in this region can lead to various spectral distortions: background counts, shadow peaks, asymmetric peaks, etc. In risetime discrimination, events with a slow rise do not contribute to the spectrum but are rejected.

The DP4 implements RTD by measuring the width of the fast channel response: a slower input rise time leads to a broader fast channel output. Because a broader fast channel output also has a lower amplitude (to maintain the same net area), the DP4 measures the Half-Width, Half-Max (HWHM) of the resulting response. This measured width is compared to a preset width (the “RTD Time Threshold”) and the event is rejected if the measured width is too wide. [Note that the event can only be rejected if the Fast Channel is over threshold. See the next section for a discussion of thresholds.]

Because the fast channel is inherently much noisier than the slower shaped channel, an RTD threshold is also implemented on the shaped channel. Events which fall below this threshold (the “RTD Slow Threshold”) are not processed by the RTD and are thus accepted (unless otherwise rejected by Pileup Rejection or some other criterion). Because RTD is most often needed on interactions deep in a detector, arising from high-energy events, low-amplitude events are unlikely to benefit from RTD rejection. These fall below the RTD Slow Threshold and are thus accepted.

To summarize the RTD rules:

a. Events whose shaped (slow) channel amplitude is below the RTD Slow Threshold are kept; otherwise…

b. Events whose fast channel amplitude is below the fast threshold are rejected; otherwise…

c. Events whose measured HWHM is wider than the RTD Time Threshold are rejected.

1.3.3.3 Thresholds

Slow channel threshold: The DP4 uses the Slow Channel Threshold to distinguish between events that should be added to the stored spectrum and those that shouldn’t. Events with an amplitude lower than the Slow Channel Threshold are ignored – they do not contribute to the stored spectrum. The slow channel threshold is the equivalent of a low-level discriminator (LLD).

Fast Channel Threshold: The Fast Channel Threshold is used for two functions: Rise Time Discrimination (RTD), as described in section 1.3.3.2, and Pile-up Rejection (PUR). The DP4 can only reject piled-up events if both events fired the fast channel; therefore, it is usually desirable to set the Fast Channel Threshold as close to the noise as is practical. This is discussed in more detail in later sections. If RTD and PUR are not used, then the fast channel threshold is not important.

1.3.3.4 Gate

The gate input is used with external circuitry to determine if events should be included or excluded from the spectrum. The gate can be active high or active low (or disabled). If disabled, then this input is ignored and all events (which meet the criteria above) are counted. If active high (low), then if the gate input is high (low), the event is counted in the spectrum. When counts are gated off, the clock is also gated off so that an accurate count rate can be determined.

The timing of this gate input is important. If the gate input is active while the fast channel threshold is triggered, then the event is counted as a fast count. If the gate input is active when the peak detect is triggered, then the event is counted as a slow count and shows up in the spectrum. Note that the fast and slow channels are triggered at different times, since they have different shaping times. We recommend that the gate input duration be equal to or greater than the sum of the peaking and flat top durations.

1.3.4 Multichannel Analyzer

The MCA portion of the DP4 supports 256, 512, 1024, 2048, 4096 or 8192 channels. (8192 channels is only available via the USB interface – it is not supported via RS232.) The DP4 uses 3 bytes per channel, which allows up to 16.7M counts per channel. The MCA has two spectral buffers available, A and B, which can be selected either via software, or by a hardware signal.

1.3.5 Single Channel Analyzer

The DP4 contains eight single channel analyzers (SCAs). Each SCA has an upper and a lower threshold. If an event occurs with a shaped output within the range defined by these thresholds, then a logic pulse is generated and is output to the JP9 connector on the DP4, where it can be connected to external hardware. The upper and lower limits of the 8 SCAs can be set independently in the software. SCA8 serves a dual purpose – not only does it operate like the other SCAs, but it is also used to set the Region-of-Interest (ROI) for the Preset Count mode of MCA operation. That is, when a Preset Count is selected, the MCA will stop after the programmed number of counts occurs in the SCA8 ROI.

1.4 DP4 INTERFACE

There are two distinct components to the DP4 software. The microcontroller on the DP4 contains embedded software that controls data acquisition and the interface. The computer to which the DP4 interfaces must contain software to communicate via the serial port (USB or RS-232). The current revision of the DP4 is designed primarily for use in OEM applications, embedded in an end-user's product. As such, the user may access the embedded software to tune the instrument for his/her application. Further, the personal computer software that is supplied is essentially a demonstration program. It permits the user to fully access the DP4 functionality and can be used as is, but more importantly it shows how to carry out the various functions. We presume that the user will tailor this software to meet the specific requirements of his/her application.

The DP4 has both a USB interface and a standard RS232 interface. Specifically, it has a full-speed (12Mbps) USB 1.1 interface (which is also compatible with newer USB 2.0 ports.) Amptek has licensed a USB device driver for use with Windows 98, Windows ME, Windows NT, Windows 2000 and Windows XP, which makes it easy to write Windows software to communicate with the DP4.

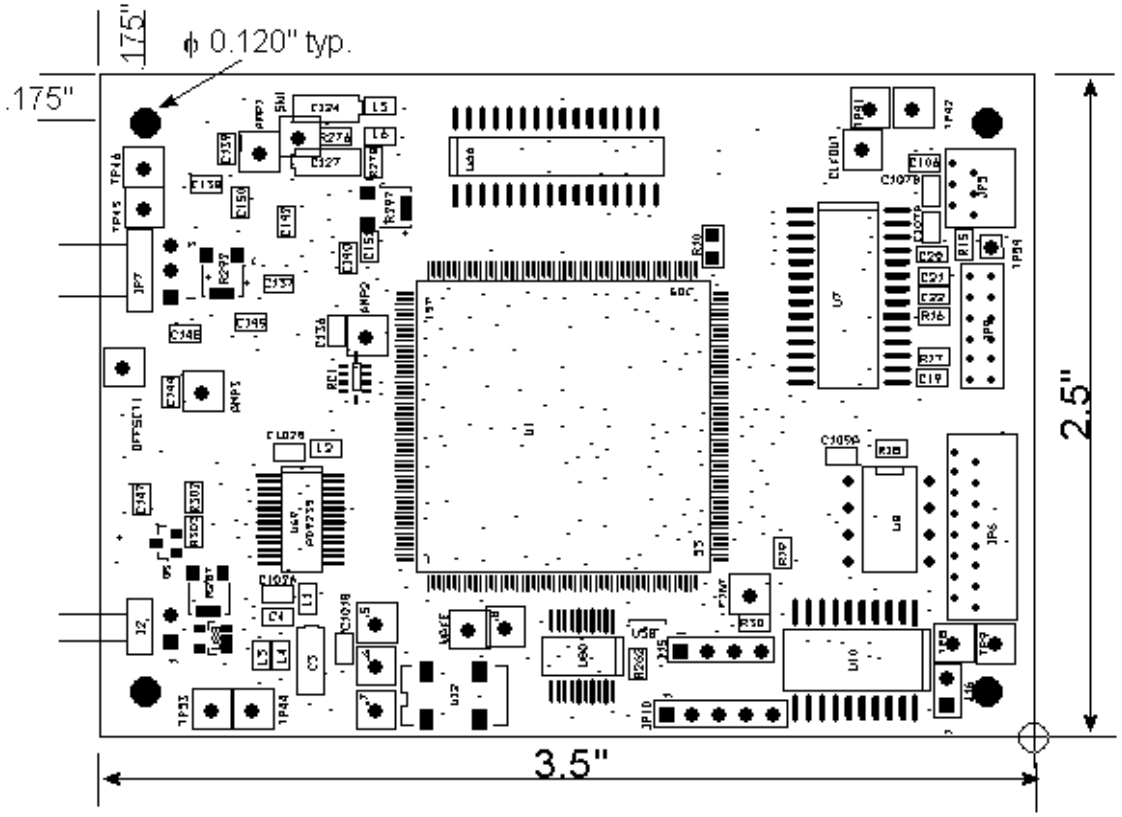
Note on the USB device driver

The USB device driver is licensed from Andrew Pargeter & Associates (www.devicedriver.com) for the Amptek DP4. The license agreement allows Amptek to provide the driver to the OEM, and the OEM to provide the driver to the end user provided that the embedded code doesn't change. In practice, an OEM who wishes to write his own embedded code will either need to relicense the USB driver or find another driver solution. If the OEM wishes only minor changes to the existing embedded code, he should contact Amptek to see if the changes could be made to the standard code, and thus would be covered by the license agreement.

The USB Vendor ID (VID) and Product ID (PID) are provided to Amptek from Andrew Pargeter & Associates ("APA") as part of the license agreement. The VID (0x0BD7) is owned by APA, and the PID (0xA021) is licensed for use only with the Amptek DP4. OEMs may not use this VID/PID combination, except with the standard Amptek DP4 embedded code. Contact Amptek for more information. For more information on VIDs & PIDs, refer to the USB Implementer's Forum (www.usb.org).

2 DP4 SPECIFICATIONS

2.1 DIMENSIONS



2.2 CONNECTIONS

There are two primary connectors, which are necessary for the DP4's operation, along with some auxiliary connectors. JP7 is the analog input, which connects to a preamplifier output. JP6 contains the power supply connections and the serial interface. These are the primary connectors and are required for operation. Their use is shown graphically in Figure 6.

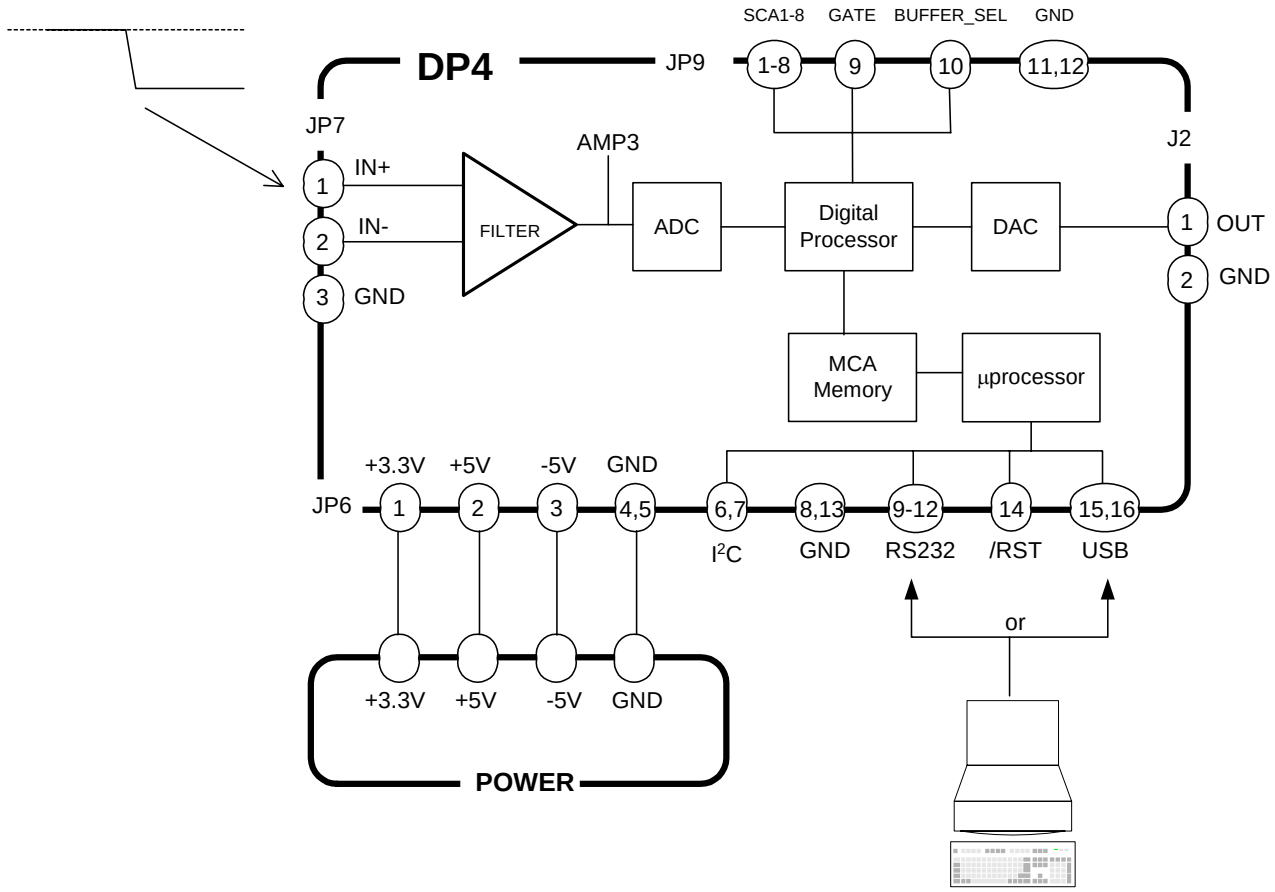


Figure 6. Block diagram illustrating the primary connections.

The auxiliary connectors include (1) an analog output, the output of a DAC, J2; (2) a proprietary test connector, JP5; (3) an external I/O connector with SCAs, GATE and BUFFER_SEL, JP9; and (4) a user connector, JP10, which is tied to four microcontroller pins.

2.2.1 JP7 – Analog input

This is the input to the DP4 from a preamplifier. +IN and –IN form a differential input to the DP4, which is an inverting amplifier.

- Pin 1: +IN: Non-inverting input. For negative pulses, connect signal to +IN and return to –IN.
- Pin 2: -IN: Inverting input. For positive-going pulses, connect signal to –IN and return to +IN.
- Pin 3: AGND: Analog ground.

Connector:

- The JP7 connector on the DP4 is a Molex P/N 22-05-3031. Mating connector is: Molex P/N 22-01-3037 (Digi-Key P/N WM2001-ND) with Molex crimp terminals P/N 08-50-0114 (Digi-Key P/N WM1114-ND).

Requirements:

- Polarity: The DP4 is an inverting amplifier. Measured at Pin 1 referenced to Pin 2, the input pulse should be negative. The connector should be wired to achieve this as discussed above.
- Magnitude: The inputs to the first amplifier stage have a common mode range of $\pm$7.6V, with a differential mode range of $\pm$3.8V. By default, a 25% attenuator is installed (R291=R296=330 ohms) to increase the common mode range to $\pm$9.5V and the differential mode range to $\pm$4.75V. If this increased range isn't needed, the attenuator can be removed (R291=R296=0 ohms). See section 2.3.1.

- The default configuration is for reset preamps. For continuous feedback preamplifiers, the hardware will require reconfiguration, as discussed in Section 0.
- Risetime >100 nsec

2.2.2 JP6 – Power and Interface

JP6 is a 16-pin 1mm flex connector.

Pin #	Name	Pin #	Name
1	+3.3V	9	RS232-RX
2	+5V	10	RS232-TX
3	-5V	11	RS232-CTS
4	GND	12	RS232-RTS
5	GND	13	GND
6	I^2C SDA	14	/RESET
7	I^2C SCL	15	USB-
8	GND	16	USB+

Table 2. Pinout for JP6, the primary power and serial interface connector

- +3.3V: This supply powers the majority of the DP4. Average operating current is 100-200mA, depending on configuration. Peak current is 500 mA at startup.
- +5V, -5V: These supplies power the analog front end. Average operating current is 10 mA for each. These should be well filtered, since ripple is likely to degrade performance. There is no overcurrent or reverse voltage protection implemented on the DP4.
- SDA, SCL: These are the I^2C bus signals. The DP4 microcontroller is the bus master, so any peripherals connected to the I^2C bus must be slaves. The only I^2C devices on the DP4 (other than the μC) are the 24AA64 boot prom and a temperature sensor.
- RS232-RX, RS232-TX, RS232-CTS, RS232-RTS: These are RS232 signals for interfacing the DP4 to a host system. The signal names are relative to the DP4, i.e. the DP4 receives on the RX pin and transmits on the TX pin. The handshaking signals CTS and RTS are not used but are available for custom applications.
- /RESET: Pulling this signal low will hold the entire DP4 in reset. Floating it or pulling it high allows normal operation.
- USB+, USB-: This is the USB (Universal Serial Bus) communication bus. The DP4 microcontroller contains a USB communication core.

Connector:

- Connector: 16 position right angle, Hirose Electronic Co. Ltd: FH21-16S-1DS, Digi-Key: HFG16T-ND
- Mating cable: 1mm Flat Flex Cable 4", Parlex: 100-16-102B, Digi-Key: HF16U-04-ND (other lengths are available)

2.2.3 J2 – Analog output

This is the shaped output from the DAC. The decimated input and other diagnostic signals can also be output from the DAC.

- Pin 1: +OUT: This is the output of the DAC. Output range is 0-1V.

- Pin 2: AGND: Analog ground. Care should be taken in connecting this ground externally, as ground currents can disturb the analog front end.

Connector:

- The J2 connector on the DP4 is a Molex P/N 22-05-3021. Mating connector is: Molex P/N 22-01-3027. (Digi-Key P/N WM2000-ND) with Molex crimp terminals P/N 08-50-0114 (Digi-Key P/N WM1114-ND)

2.2.4 JP9 External Logic I/O

JP9 is an 8x2 2mm header, which offers functionality which is required by some but not all users. Pins 1 through 8 are the outputs of the single channel analyzer outputs, discussed in section 1.3.5. Pins 9 and 10 are the gate input (section 1.3.3.4) and buffer select input (section 2.3.4), respectively. Pins 11 and 12 are ground.

Pin	Function	Pin	Function	Pin	Function
1	SCA1	5	SCA3	9	GATE IN
2	SCA8	6	SCA6	10	BUFFER SEL
3	SCA2	7	SCA4	11	GND
4	SCA7	8	SCA5	12	GND

GATE and BUFFER_SEL inputs:

V_{IL} (logic low): -0.5 to + 0.7V V_{IH} (logic high): +2.4 to +5.5V

Inputs: SN74LVC2G14, Vcc=3.3V, 100 kΩ pull-downs

SCA Outputs:

V_{OL} (logic low): 0.1V @ 100uA V_{OH} (logic high): +3.1V @ 100uA

Outputs: SN74LVC245A, Vcc=3.3V, 49.9 Ω series termination

Pulse width: 50nS

2.2.5 J15 I^2C Bus

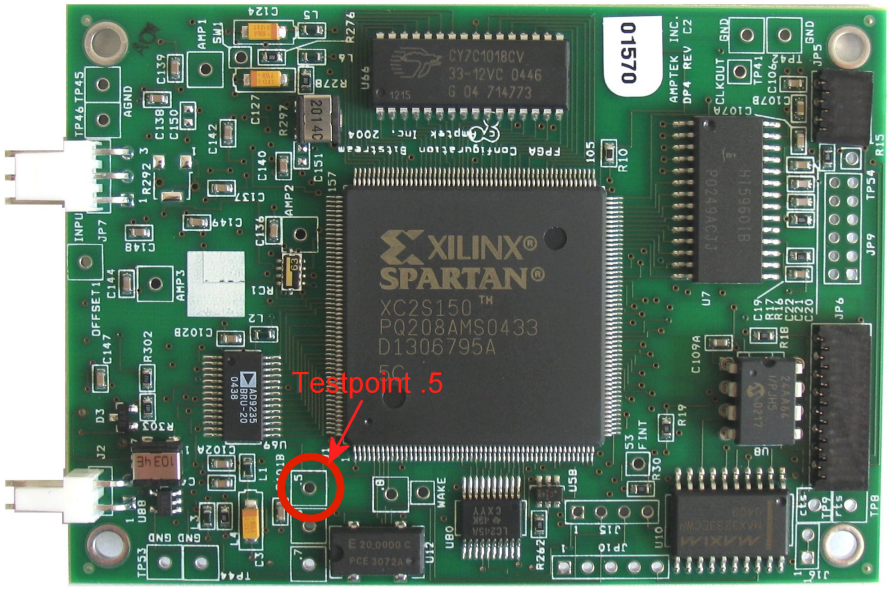
J15 includes the I^2C bus signals (SCL & SDA), and a global active low reset input (/RESET). This header can be used for in-circuit programming of the microcontroller EEPROM, or it can be used by custom applications to communicate with other I^2C devices.

2.2.6 Diagnostic Testpoint .5

The DP4 has a diagnostic testpoint, labeled '.5', which is located near the FPGA (see picture below). This testpoint can be configured via the application software to output a number of useful signals, as listed below:

Signal Name	Function
ICR	Input Count Rate, i.e. Fast Channel fired
PILEUP	Piled-up event detected
HOLD	(Internal diagnostic)
ONESHOT	Period during which a 2nd event would be considered piled-up
DET_RES_	Active-Low Detector Reset Lockout Period

MCA_EN	High=MCA Enabled, Low=MCA Disabled
TRIGGER	Peak Detect Fired
SCA8	Single Channel Analyzer output #8 (Also available on JP9)



2.2.7 JP10 Extra signals for OEM use

JP10 contains signals from four unused pins on the microcontroller. These pins are configured as outputs, and can be controlled via USB commands (See section 5.2.1). The outputs go between 0V (0.4V @ -1.6mA) and +3.3V (+2.4V @ 1.6mA).

Pin #	Function
1	Output #1
2	Output #2
3	Output #3
4	Output #4
5	GND

2.3 CONTROLS AND ADJUSTMENTS

2.3.1 Analog Prefilter

- Inversion: On JP7, pins +IN and –IN form a differential input. The DP4 requires a negative pulse on +IN relative to –IN.
- Input Attenuation: If the signal exceeds the nominal range of +/- 3.8V, R291 & R296 can be used to attenuate the input signal. R291=R296=330 ohms yields 25% attenuation (the default configuration); 1Kohm yields 50% attenuation.

- Coarse Gain: Four coarse gain settings are available, by command from the microcontroller. The gain settings are x10.8, x20.7, x55.4, and x106.2.
- Fine Gain: Fine gain is adjusted digitally, via software, over a range of +/- 25%.
- Offset: The pot R287 sets the DC offset into the ADC. The ADC input should never drop below zero, or significant distortions in the pulse shape will occur.
- Input Pole: The pot R297 is used to set an input pole, part of the prefilter function.

2.3.2 Pulse Shaping

- Rise and Fall Time: The rise time of the shaped pulse, which must equal the fall time, can be set to any one of several values, listed in Table 1. This is adjusted digitally: the microcontroller writes the desired value to a register in the pulse shaping hardware. The demonstration software provides a simple control for this. Setting this value by the demonstration software is described in sections 3.2.2 and 4.
- Flat Top Duration: The duration of the trapezoidal flat top can also be set to one of several values, by a digital command.
- Decimation: For long rise times, the input ADC values are decimated, as is common with digital processing. The decimation setting is related to the rise/fall time and the flat top duration. This is also set by digital command.
- DAC Controls: The DAC has several controls, described more fully in section 5. The DAC provides an analog display of the digital processing that is occurring. The analog display is not needed but is convenient for setup and debugging. First, the DAC can be enabled or disabled. Second, several different waveforms may be sent to the DAC. This includes the fast channel output, the decimated input, the shaped output, and the BLR correction. Third, a DC offset can be sent to the DAC. The DAC responds to underflows (outputs below 0V) by wrapping over, so it is recommended practice to set a DC offset that avoids this.
- Preamp Reset Controls: These are utilized with reset type preamps and their operation is described in section 1.3.2.1. The user may enable or disable Autobaseline. The user may also set a reset period, which is the length of time following a reset signal during which data processing is shut down, to permit the electronics to fully recover. The user may also elect to disable reset detection. These controls are sent by software to the pulse processing FPGA.
- Baseline Restoration Controls: The operation of the baseline restorer is described in section 1.3.2.2. The user may enable or disable BLR. If enabled, then the user may choose to set three parameters: up, down, and threshold, each set to one of four values. “Up” (“Down”) determines the size of the upward (downward) step to the baseline. “Threshold” determines when an upward correction is required. These controls are sent by software to the pulse processing FPGA. Autobaseline should be disabled if BLR is enabled or if a non-reset style preamp is used.

2.3.3 Pulse Selection

- Fast Threshold: A low level threshold for the fast channel can be set by a digital command. The logic output is used in subsequent pulse processing.
- Pile-Up Rejection: The pile-up rejection (PUR) has one direct control, the on/off control. Indirectly, the operation of the PUR is greatly affected by the setting of the Fast Channel Threshold. Only signals with a fast channel response exceeding this threshold are evaluated for possible pile-up. If this threshold is set too low, then electronic noise triggers the PUR detect circuits. Pulses are rejected if they occur close in time with noise, and therefore there is very low data throughput. If this threshold is set too high, then real events are missed and therefore pile-up will be present in the spectrum. Common practice is to set the fast threshold to generate 5-10 cps, in the absence of any signal, which puts this level as close to the noise as possible without degrading throughput.
- Pile-up period: the pile-up period (the minimum interval between two successive peaks which are not considered piled up) is programmable. The optimal setting is:

  (RisetimeRegister * 19 + (FlatTopRegister + 1) * 4) / 2.

- Risetime Discrimination: Risetime discrimination is described in section 1.3.3.2. There are three controls, each sent via software to the FPGA. First, RTD may be enabled or disabled. Second, if enabled, then the user may set the threshold. This threshold applies to the slow channel. Only events exceeding this threshold will be analyzed by the RTD circuit; all events below this threshold are accepted. Third, the user may set the HWHM for the fast channel. Only events with a HWHM below this value will be accepted.

2.3.4 MCA Control

- Number of channels: The MCA can be set to have 256, 512, 1024, 2048, 4096, or 8192 channels.
- Slow Channel Threshold (LLD): As with most MCAs, there is a low level discriminator on the slow channel. Only pulses exceeding this threshold will be recorded in the MCA spectrum. The register setting of 0-255 corresponds to about 0-25% of the full-scale output.
- Gate: In software, the user may set the gate “off”, in which case the gate input is ignored. The user may also set it to active high or active low.
- Buffer: There are two memory buffers in the hardware, designated A and B. The user may choose to use either. In addition, the user may choose to enable “Hardware Select”. If this is enabled, then an external logic input controls whether the data go into buffer A or B.
- Preset Time: The accumulation time may be preset, from 100ms to 19.4 days, with 100ms precision. This is set in software. After this time has elapsed, acquisition will stop. This will be the accumulation time, the duration of data acquisition, not live time and not elapsed clock time. See section 7.3 for details on accumulation time.
- Preset Counts: The DP4 can be programmed to acquire a preset number of counts in a region of interest. Acquisition will stop when this number of counts is reached. SCA8 must be configured with the region of interest.

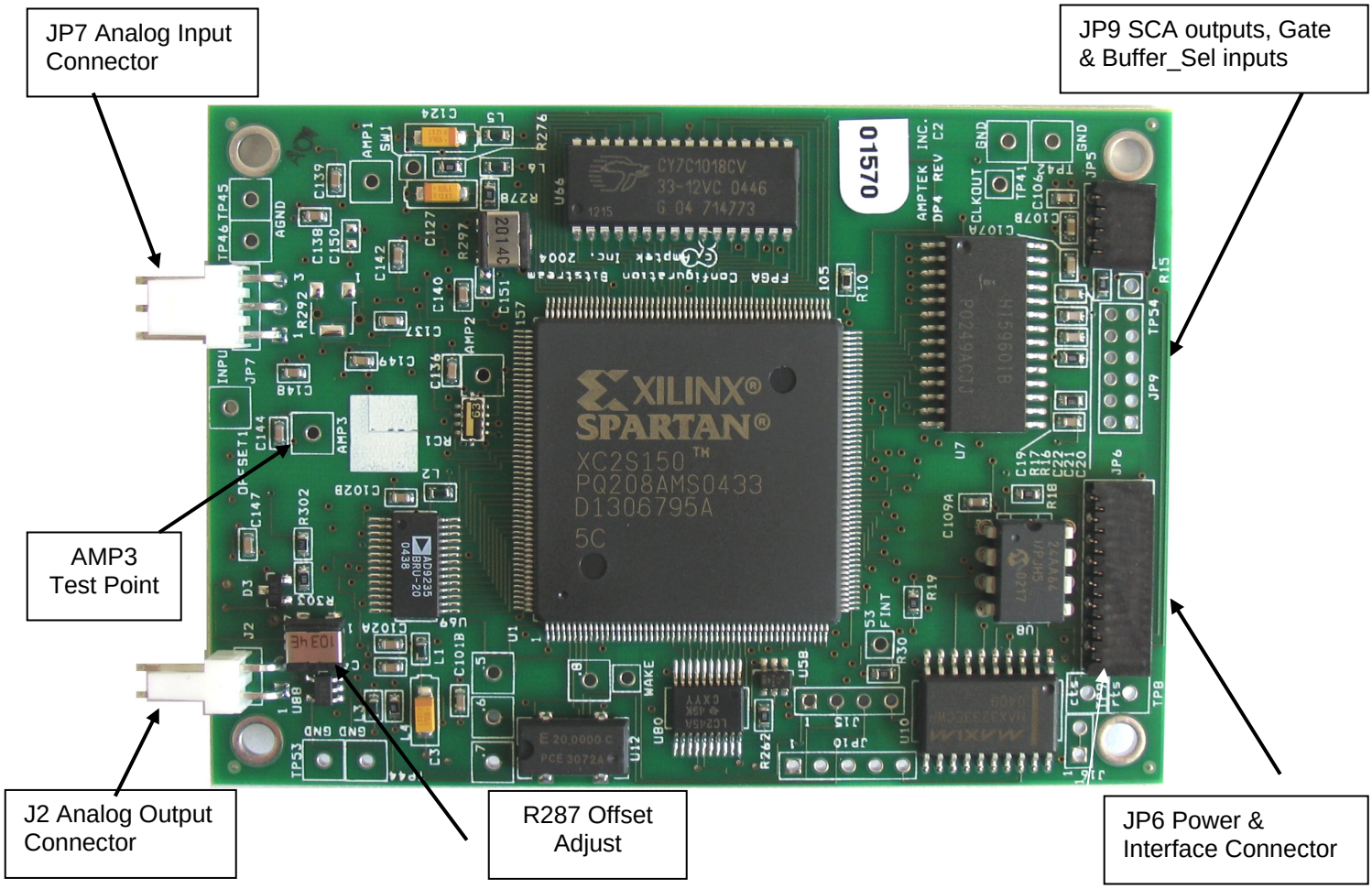
2.3.5 SCA Controls

There are 8 SCA channels, each of which has the following three controls.

- Enable: If this is selected, then that channel outputs counts.
- Lower and Upper Thresholds: These define the range of the SCA. These are in MCA channels: if the MCA is is 1024 channel mode, and SCA 1 has a range of 712 to 800 for example, then any time a count is binned in this range of MCA channels, there will be a logic pulse on the SCA output.

3 QUICK START INSTRUCTIONS

The purpose of this section is to provide enough information to set up the DP4 hardware, install the demonstration software, and start taking data. More detailed information on the hardware and software is elsewhere. In particular, the interface software which runs on the personal computer is described in more detail in section 4. The most important connectors and controls are shown below.



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3.1 SET-UP INSTRUCTIONS

3.1.1 Software installation and serial port connection (USB)

1) All of the necessary software is on the CDROM. Run the 'setup' program in the DP4 folder to install the compiled Visual Basic software. [The Visual Basic source code is in the 'Source Code\VB' folder]

2) Connect the USB interface, per section 2.2.2 on page 13, to the USB port of a personal computer or hub. [A USB 'A' to 'B' cable is required to connect between the USB connector on the optional DP4 connector or power supply boards (PC4-1,2,3) and the USB port of a PC or hub.] Apply power to the DP4; the 'New Hardware Wizard' should automatically start on the PC. Follow the directions below to install the USB device driver, depending on which version of Windows is in use.

3) For Windows 2000 or Windows XP:

    a. In the "Found New Hardware Wizard" (which should automatically appear when the DP4 is connected and powered on for the first time), select "Install from a list or specific location", and click "Next >".

    b. Select "Don't Search. I will choose the driver to install." and click "Next >".

    c. Click the "Have Disk…" button.

    d. Select "Browse…" and navigate to the \USB_driver\Win2K_XP folder of the DP4 CDROM. Select "OK".

    e. Click "Next >".

    f. Click "Finish". The USB driver should now be installed.

4) For Windows 98 or Windows ME:

    a. The "Add New Hardware Wizard" should automatically appear when the DP4 is connected and powered on for the first time. Click "Next >".

    b. Select "Search for the best driver for you device" and click "Next >".

    c. Select only "Specify a location:", click "Browse" and navigate to the \USB_driver\Win98_ME folder of the DP4 CDROM. Click "Next >".

    d. Windows is now ready to install the driver. Click "Next >".

    e. Click "Finish". The USB driver should now be installed.

Note for users of the original DP4: The original DP4 only supported up to 4096 channel spectra, and therefore the USB driver was configured to not allow transfers larger than that. The DP4 Rev. C now supports 8192 channel spectra, which may not work properly with the previous driver configuration if the DP4 is configured for 8192 channels. There are 2 solutions: 1) Uninstall the USB driver, and reinstall as described above. 2) Edit the registry entry which limits the transfer size to 4096 channels. Please contact Amptek for guidance if this issue affects you.

3.1.2 Software installation and serial port connection (RS232)

1) All of the necessary software is on the CDROM. Run the 'setup' program in the DP4 folder to install the compiled Visual Basic software. [The Visual Basic source code is in the 'Source Code\VB' folder]

2) Connect the RS232 interface, per section 2.2.2 on page 13, to the serial port of a personal computer. The RS232 handshaking lines RTS & CTS don't need to be connected unless custom software is used. Amptek offers several different DP4 power supply solutions (PC4 interface boards) which include standard RS232 connectors.

3.1.3 Hardware connections

1) Connect the power supply and the RS232 or USB interface, per section 2.2.2 on page 13. The +3.3V, +/-5V, GND, and RS232 or USB lines must be connected. We recommend verifying the voltages and current limits of the power supply before connecting to the DP4. The RS232 lines should connect to the

serial port of a personal computer; the USB lines can connect to the USB port of a PC or to a USB hub. [The RS232 handshaking lines RTS & CTS don't need to be connected unless custom software is used.]

2) Connect the preamplifier output to the DP4 input JP7, per section 2.2.1 on page 12.

3) Connect the DP4 analog output J2, per section 2.2.3 on page 13, to an oscilloscope. Although this output from the DAC is not required for operation, it is recommended during initial set up. Use jumper pins 1 and 2 of JP8 to enable the DAC.

3.1.4 Power On

1) Turn on the detector and preamplifier and place an appropriate radioactive source in front of the detector. It may be useful to verify, using an oscilloscope, that the preamplifier is producing signals of the correct size and polarity.

2) With the computer on, double click on the PX4.EXE icon. The screen should look as below. The CONFIGURE button will be yellow when the user has made changes to the configuration on the screen but not yet sent the new configuration to the DP4.

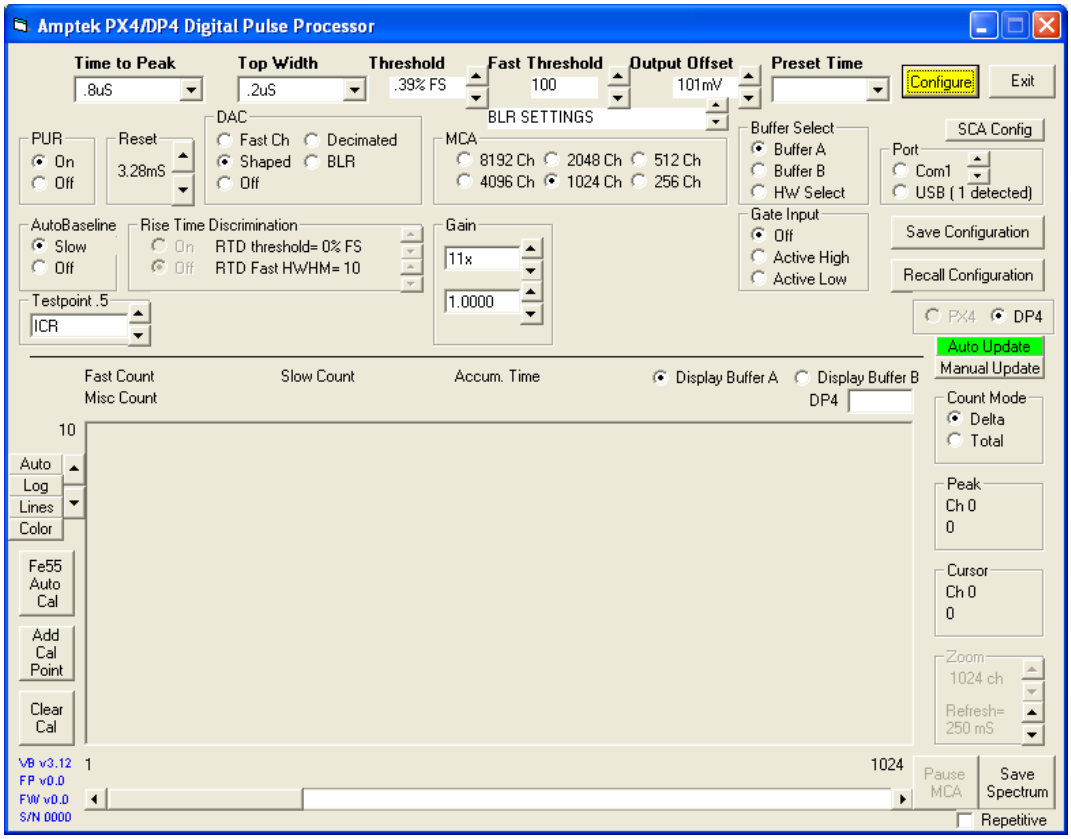


Figure 7. Graphical User Interface for the demonstration data acquisition and control software, which is written in Visual Basic v5.0.

3) Turn on power to the DP4. The +3.3V line should draw 100 to 180 mA, while the +/-5 V lines should draw <10 mA. No output should be visible on the screen or on the oscilloscope until the unit has been configured.

4) For quick operation, select the proper communications port (COM1, COM2 or USB) on the screen and then click on CONFIGURE, which will turn from yellow to gray. This is not necessarily the optimum configuration but will make the unit operate.

5) You can confirm that the DP4 & PC are communicating by checking the lower left-hand corner of the screen. 'FP' (FPGA version), 'FW' (Firmware version) and S/N (Serial Number) will become non-zero when communication is established.

3.2 CONFIGURING THE DP4

3.2.1 Adjustments via hardware

1) Connect an oscilloscope probe to the test point labeled AMP3. The signal should look like the traces shown previously, as the "analog prefilter output" in Figure 4.

2) The pulses of interest should have a magnitude of approximately 1V, with an offset of 100 to 200 mV. The offset must be large enough that the signal normally does not drop below ground – it can go below ground during detector reset.

   If the polarity is incorrect, refer to section 2.3.1. The coarse gain is adjusted via software, as discussed below. If the signal amplitude is too large, with the coarse gain at its minimum, set the input attenuator as described in section 2.3.1. If the offset is incorrect, adjust R287.

3.2.2 Adjustments via software

The following parameters can be set via the Visual Basic Software, using the graphical interface shown in

Figure 7 on page 20. Note that the changes are communicated to the DP4 and thereby take effect when the CONFIGURE button is clicked.

1) Set the **Time To Peak**, using the pull-down in the upper left hand corner. The peaking time corresponds to about 2.4 times the shaping time of a pseudo-gaussian shaper. Any one of the values between 0.8 and 102.4 μsec can be chosen. Once the time to peak has been chosen, the duration of the flat top can be chosen. The range of allowable values is determined by the time to peak.

2) Set the **Analog Gain**, using the group of buttons near the middle of the screen. The top box determines coarse gain and allows any of the four values. A gain of 100 will lead to a full-scale energy of approximately 10 keV, using an Amptek XR-100, but this is very approximate and a full calibration should be used. The lower box determines fine gain. The user may use the arrows or may type a new value in the box (configure must be pressed after this).

3) Set the **Threshold**. The Threshold setting corresponds roughly to an LLD (low level discriminator) on an MCA. If the peak height of the shaped pulse in the slow channel is below this threshold, it will not be binned in the histogram. The number, e.g. 1.07% FS, corresponds to 1.07% of the full scale in MCA channels. If this threshold is too low, then only low amplitude noise counts will appear on the screen.

4) Set the **Fast Threshold**. The Fast Threshold setting applies to the fast signal used for pile-up rejection. Only signals exceeding this threshold can activate the pile-up reject. If this is set too low, then noise activates the pile-up reject, rejecting an excessive number of actual signal counts. If set too high, then piled up events might not be rejected.

5) For reset preamps, set Autobaseline to "Slow" and Reset to the longest, 13.1 msec. For continuous feedback preamps, set Autobaseline to "Off", Reset to "Off", and set the BLR to some value. Dn 16, Up 16, and Th 256 is often a good starting point.

6) **For simplicity, we recommend turning off the various data processing options initially. Set PUR off, RTD off, Gate Input Off. Experience has shown this to be very useful for initial setup and debugging.**

7) Set the DAC to "Shaped". Set the **Output Offset**. This commands a DC offset voltage to the DAC, for display on the oscilloscope. It will have no effect on the spectrum displayed in Visual Basic. If the offset is too low, then the output will sometimes go below zero. The DAC is unipolar and therefore it wraps over, leading to a large voltage. A recommended value is 100 mV.

8) After setting these to approximate values, click Configure. The output pulse shape and the spectrum should be close to their desirable values. These parameters can be refined.

3.3 TAKING DATA

1) To accumulate a spectrum for an extended period, select **Count Mode Total**. The counts in the spectrum will integrate over time. By default, the plot autoscales.

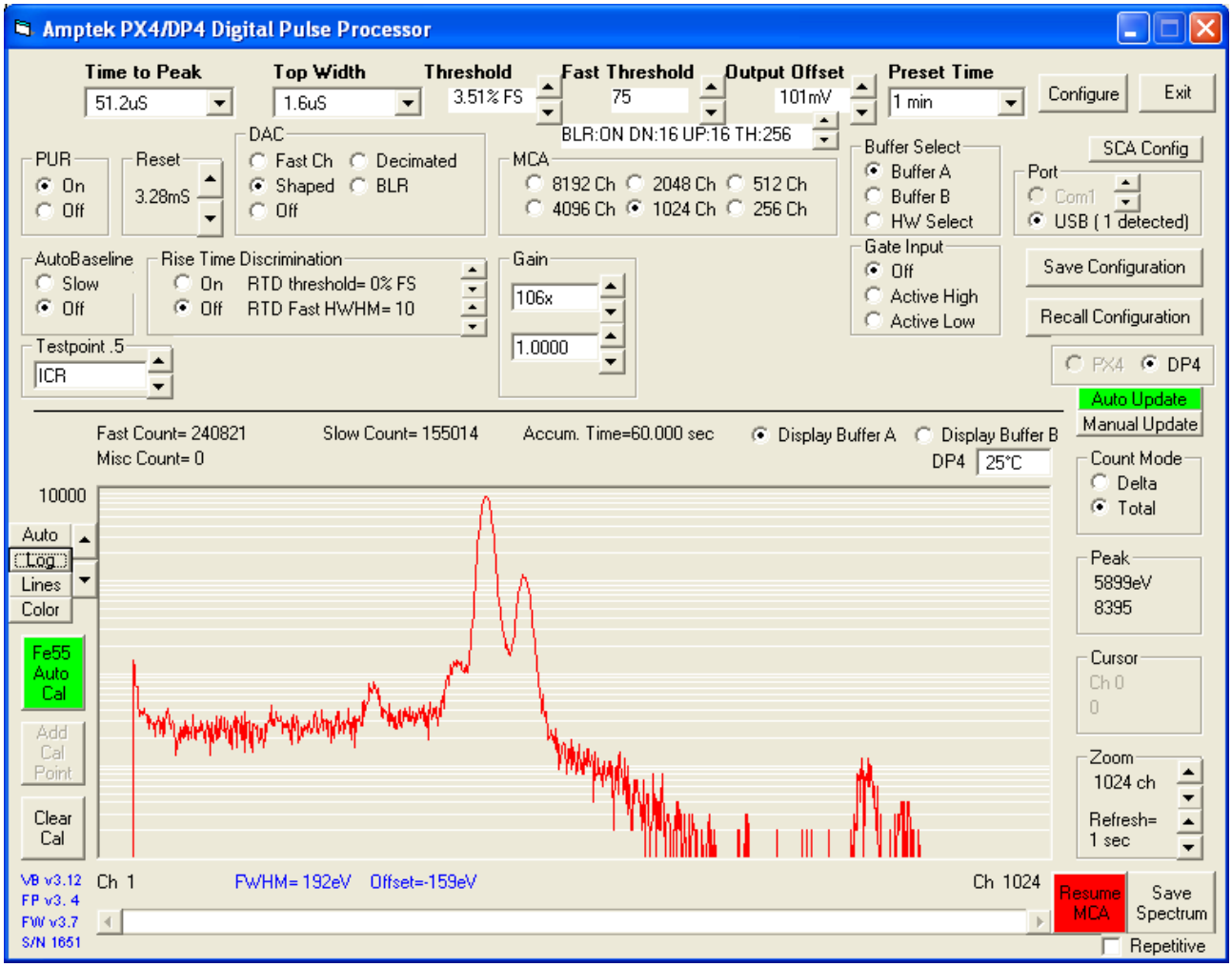
2) To clear the spectrum, set Count Mode to Delta for an accumulation, then set it back to Total.

3) To save data, select the **Save Spectrum** button. The user will be prompted for a file name. The file is written in the standard format of Amptek's PMCA software. This is an ASCII format, with several lines of header information, followed by the spectrum, with one line per channel. It can be read using Amptek's PMCA software or by any software which reads ASCII, e.g. Excel or WordPad.

For further information regarding this interface software, please refer to section 4.

4 CONTROL AND DISPLAY DEMONSTRATION SOFTWARE

A demonstration user interface program is supplied with the DP4. This software is fully functional, permitting the user to access all of the parameters and features of the DP4. It is intended to demonstrate how to interface with and use the DP4. There are some new controls available for the DP4 Rev. C: The fine gain (set to 1.0000 here), the SCA config button, and an 8k channel selection for the MCA.



- Time to Peak: Sets the peaking time for the shaped pulse.
- Top Width: Sets the width of the trapezoidal flat top for the shaped pulse.
- Threshold: Sets the lower threshold for spectrum accumulation. Works like an LLD on an MCA.
- Fast Threshold: Sets the threshold for the fast channel pile-up reject logic. If this threshold is too low, then valid counts are rejected by noise, leading to a very low throughput.
- Output Offset: The offset voltage of the DAC. Should be high enough to prevent underflow.
- Configure: Sends the configuration parameters from the PC to the DP4. If this is yellow, then configuration parameters have been changed in the PC and not yet sent to the DP4.
- Exit: Exits the program.
- PUR: Enables or disables pile-up reject.
- Reset: Sets the duration of the lockout interval following a reset pulse from the preamplifier.

- DAC: Selects which signal is sent to the DAC. If the DAC is off, power consumption is reduced.
- MCA: Selects the number of MCA channels to be used.
- Buffer Select: May use memory buffer A or B, or enable hardware selection of the buffers.
- SCA Config: Clicking on this button will bring up another window, with the SCA controls. In this window, each of the eight SCAs has an enable check box, a lower level, and an upper level. The 'Preset Counts' setting is also found here (it uses the ROI for SCA8.)
- Port: Selects PC serial port COM1-COM8 (for an RS232 interface), or USB Port (for the USB Interface).
- AutoBaseline: Enables AutoBaseline.
- Risetime Discrimination: Turns RTD on, and sets the amplitude and timing thresholds.
- Analog Coarse Gain: Selects one of 4 gain settings. A setting of 100 (10 keV) implies that the full-scale energy will be approximately 10 keV, using an Amptek XR100.
- Digital Fine Gain: Sets the gain to a range of 0.75 to 1.25 in steps of ?? 0.001.
- Gate Input: Enables Gate and selects active High or Low.
- Save/Recall Configuration: Saves or recalls the configuration parameters set in this software. The configuration file is named 'DP4.CFG' and is stored in the current folder.
- Fast Count: Displays the number of counts that have accumulated in the fast channel in the present data acquisition interval.
- Slow Count: Displays the number of counts that have accumulated in the slow channel in the present data acquisition interval.
- Accumulation Time: Displays the duration (real time) of the present data acquisition interval.
- Auto/Manual Update: In Auto update mode, the PC periodically queries the DP4 and downloads the spectrum. In Manual Update mode, the data are only transmitted from the DP4 when the user selects the manual update button. In auto update with the RS232 interface, the update rate is a function of MCA channels: 4 sec for 4096 channels, 2 sec for 2048 channels, 1 sec for 1024 channels, 500 msec for 512 channels, and 250 msec for 256 channels. (8192 channel mode is not supported via the RS232 interface.)
- Count Mode: In Delta mode, the spectrum only displays counts received in the most recent data update interval (i.e., 1 second). The histogram memory is cleared after each update. In Total mode, counts are integrated. Integration begins at the end of the update when Total was pressed and continuous until the update after Delta was pressed. Selecting Delta mode is used to clear the spectrum. (Note: the integration takes place in the DP4, not the host PC.)
- Peak: Indicates the MCA channel with the maximum number of counts, and the number of counts in that channel.
- Cursor: Indicates the MCA channel selected by the cursor and the number of counts in that channel (Left-click with the mouse to set the cursor. The right & left arrow keys move the cursor when the graph is selected.)
- Zoom: Permits the user to zoom in on a subset of the MCA channels. For the RS232 interface, only the selected channels are sent from the DP4 to the host PC, which allows a faster refresh rate. For the USB interface, the DP4 always sends the entire spectrum.
- Save Spectrum: Saves the spectrum to a file. The user will be prompted for a file name. The file is written in the standard format of Amptek's PMCA software. This is an ASCII format, with several lines of header information, followed by the spectrum, with one line per channel. It can be read using Amptek's PMCA software or by any software which reads ASCII, e.g. Excel or WordPad. When saved as a PMCA file the data can be processed by the XRF-FP Quantitative analysis software.

- Scale: Sets the vertical scale for spectrum display. By default, the software uses autoscaling based on the maximum counts. The user may also manually scale. Scaling can be either linear or logarithmic.
- 55Fe Auto Cal: Provides a convenient automatic calibration, assuming an ^{55}Fe source is used. Selects appropriate peaks for the 5.9 and 6.4 keV lines and performs a simple, two-point calibration. (For this to function correctly, the ^{55}Fe peaks must be the highest peaks in the spectrum.)
- Add Cal Point: Permits the user to add additional calibration points for a linear regression.
- Pause MCA: Manually starts and stops data acquisition. Only functional with USB.

At the bottom left hand corner of the window is a series of three numbers. These track the configuration of the system at the time this manual was written. VB v3.13 is the version of the Visual Basic display software in use. FP v3.4 is the version of the FPGA in use. FW v3.8 is the version of the embedded software in use.

5 PROGRAMMER'S GUIDE

5.1 RS232 SERIAL INTERFACE

The DP4 uses the RS232 at 57.6kbaud, with 1 start bit, 8 data bits, 1 stop bit and no parity. No hardware or software handshaking is used. Note that there are no checksums or other checking.

There are two types of data transfers between the DP4 and the host: a configuration packet, and a data request packet. The DP4 will respond to a configuration packet by immediately updating its configuration. It will respond to a data request packet by sending 256 bytes of data.

The configuration packet via RS232 consists of the 64-byte USB configuration packet (described in section 5.2.2), preceded by a sync byte, and followed by an end byte, for a total of 66 bytes.

Byte 1 0xFD (sync)
Bytes 2-65 are identical to the 64-byte USB Configuration packet (see Section 5.2.2)
Byte 66 0xFE (end of config packet)

NOTE: none of the configuration bytes can have the value 0xFD, 0xFE, 0xFF.

Data request packet (3 bytes):

Byte 1 0xFD (sync)
Byte 2 requested packet number
Byte 3 0xFF (end of packet request)

[To tell the DP4 to clear the entire MCA buffer, add 0x80 to packet # of the last data request.] The DP4 will respond to a data request by sending 256 bytes of data.

MCA Mode	Buffer A Packet Numbers	Buffer B Packet Numbers
256 channels	0x00-0x02 (3 packets)	0x40-0x42
512 channels	0x00-0x05 (6 packets)	0x40-0x45
1024 channels	0x00-0x0B (12 packets)	0x40-0x4B
2048 channels	0x00-0x17 (24 packets)	0x40-0x57
4096 channels	0x00-0x2F (48 packets)	0x40-0x6F
8192 channels	Not supported via RS232	Not supported via RS232
Status packet	0x30	0x70

The spectral packets should be assembled in order into one buffer. The spectral data format is 3 bytes/channel, in order from LSB to MSB, and in channel number from lowest to highest.

5.2 USB INTERFACE

5.2.1 Function Calls

Following are details of the USB function calls in the Visual Basic sample application. Refer to the documentation for the APA USB driver for specifics (on the DP4 CD-ROM), and to the Visual Basic sample application source code to see how each function is used.

USBDRVD_GetDevCount (called *by btnConfigure*, *btnPauseMCA_Click*, *Timer1_Timer*, and *Timer2_Timer*)

This is called prior to opening the USB port, to be sure that a DP4 is available. It's also called prior to most DP4 USB transfers, to be sure that the DP4 hasn't been disconnected or powered off.

USBDRVD_OpenDevice (called by *btnConfigure*)

This opens the device for handle access, which is required for USBDRVD_VendorOrClassRequestOut.

USBDRVD_PipeOpen (called by *btnConfigure*)

This opens the various DP4 pipes:

USB Pipe	Pipe Function
Pipe 0	Configuration data OUT to DP4 (USB Device Endpoint OUT1)
Pipe 1	Buffer A Status IN from DP4 (USB Device Endpoint IN1)
Pipe 2	Buffer A Spectrum IN from DP4 (USB Device Endpoint IN2)
Pipe 3	Buffer B Status IN from DP4 (USB Device Endpoint IN3)
Pipe 4	Buffer B Spectrum IN from DP4 (USB Device Endpoint IN4)
Pipe 5	Configuration readback IN from DP4 (USB Device Endpoint IN5)

USBDRVD_PipeWriteTimeout (called by *btnConfigure*)

This is used to send the 64-byte configuration packet to the DP4.

USBDRVD_CloseDevice (called by *btnExit_Click* and *Timer2_Timer*)

This closes the device handle. Timer2 will close the device if it is open but USBDRVD_GetDevCount detects no DP4s, due to disconnection or powering down.

USBDRVD_PipeClose (called by *btnExit_Click* and *Timer2_Timer*)

This closes the open pipes. Timer2 will close the handles if they are open but USBDRVD_GetDevCount detects no DP4s, due to disconnection or powering down.

USBDRVD_VendorOrClassRequestOut (called by *btnPauseMCA_Click* and *Timer1_Timer*)

This sends a zero-length 'vendor request' packet to the DP4. (The packet format is described in section 5.2.2.)

The btnPauseMCA_Click routine calls it with a request of 0x82 to disable (i.e pause) the MCA or 0x83 to enable (i.e resume) the MCA.

The Timer1_Timer routine calls it after a spectrum transfer to clear spectrum buffer A (request=0x80) or spectrum buffer B (request=0x81).

There are also commands to turn ON or OFF the four general-purpose pins on JP10.

USB 'Vendor Request'	**Function**
0x80	Clear spectrum buffer A
0x81	Clear spectrum buffer B
0x82	Disable MCA
0x83	Enable MCA
0x88	Turn OFF JP10 Pin 1 (set to 0V)
0x89	Turn ON JP10 Pin 1 (set to +3.3V)
0x8A	Turn OFF JP10 Pin 2 (set to 0V)

0x8B	Turn ON JP10 Pin 2 (set to +3.3V)
0x8C	Turn OFF JP10 Pin 3 (set to 0V)
0x8D	Turn ON JP10 Pin 3 (set to +3.3V)
0x8E	Turn OFF JP10 Pin 4 (set to 0V)
0x8F	Turn ON JP10 Pin 4 (set to +3.3V)

USBDRVD_PipeReadTimeout (called by *Timer1_Timer*)

This is called to retrieve the entire spectrum from either buffer A or buffer B, or the status packet for buffer A or buffer B. The spectral data format is 3 bytes/channel, in order from LSB to MSB, and in channel number from lowest to highest. The status packet format is described in section 5.2.3.

Note: for proper operation, the calling program should request a byte count of the expected amount plus one. For example, in 1024 channel mode, a spectrum request should ask for 3073 bytes rather than 3072. A status packet request should request 65 bytes, not 64.

5.2.2 USB Configuration Packet Format

Offset	Data bits	Allowed Value	Description
0	D7	0	0=Normal reset lockout, 1=fast reset lockout
	D6-D3	t=0…15	Flat top width=200nS*(t+1)*2^d
	D2-D0	d=0…4	Decimation factor=2^d
1	D7-D0	0…255	Slow channel threshold
2	D7-D0	0…255	Fast channel threshold
3	D7-D1	-64…+63	Output DAC offset (signed) (-500mV to +492mV)
	D0	0	DAC disabled
		1	DAC enabled
4	D7-D6	0	normal operation
	D5	0	MCA disabled
		1	MCA enabled
	D4-D2	0	MCA 4096 channel mode
		1	MCA 2048 channel mode
		2	MCA 1024 channel mode
		3	MCA 512 channel mode
		4	MCA 256 channel mode
		5	MCA 8192 channel mode
	D1-D0	0	DAC output=fast channel
		1	DAC output=shaped pulse

		2	DAC output=decimated input
		3	DAC output= BLR correction
5	D7-D0	1…255	Pileup Reject interval: optimal setting is (p * 19 + (t + 1) * 4) / 2
		0	Pileup Reject disabled
6	D7-D4	p=1…8	Peaking Time=800nS*p*2^d (See Config byte 0: bits D2-D0, and also Table 1)
	D3-D2	0	Detector reset lockout period=13.11mS (slow) or 819uS (fast) (see Config byte 0: bit D0)
		1	Detector reset lockout period=6.55mS or 410uS
		2	Detector reset lockout period=3.28mS or 205uS
		3	Detector reset lockout period=1.64mS or 102uS
	D1	0	No auto baseline reset during detector reset
		1	Auto baseline reset during detector reset
	D0	0	Disable MCA during detector reset
		1	Do not disable MCA during detector reset
7	D7-D0	0…255	RTD slow threshold
8	D7	1	Normal operation
	D6-D5	0	Analog gain=10.8
		1	Analog gain=20.7
		2	Analog gain=55.4
		3	Analog gain=106.2
	D4	0	RTD off
		1	RTD on
	D3-D0	0…15	RTD time threshold
9	D7	0	50% digital attenuation
		1	Normal operation
	D6	0	0=Baseline Restoration (BLR) off
		1	BLR enabled
	D5-D4	0	BLR Down correction=very slow
		1	BLR Down correction=slow
		2	BLR Down correction=medium
		3	BLR Down correction=fast
	D3-D2	0	BLR Up correction=very slow
		1	BLR Up correction=slow
		2	BLR Up correction=medium
		3	BLR Up correction=fast

	D1-D0	0	BLR correction threshold=very fast
		1	BLR correction threshold=fast
		2	BLR correction threshold=normal
		3	BLR correction threshold=slow
10	D7-D6	0	GATE off
		1	N/A (Gate off)
		2	GATE on, polarity active high
		3	GATE on, polarity active low
	D5-D4	0	Software MCA buffer select, buffer A
		1	Software MCA buffer select, buffer B
		2	Hardware MCA buffer select
		3	N/A
	D3	0	N/A
	D2-D0	0	AUX_OUT=ICR
		1	AUX_OUT=PILEUP
		2	AUX_OUT=HOLD
		3	AUX_OUT=ONESHOT
		4	AUX_OUT=DET_RES (active low)
		5	AUX_OUT=MCA_EN
		6	AUX_OUT=TRIGGER
		7	AUX_OUT=SCA8
11	D7-D0	0-255	Preset time LSB
12	D7-D0	0-255	Preset time Byte2
13	D7-D0	0-255	Preset time MSB [Time=0.1 sec * [MSB*(2^16)+Byte2*(2^8)+LSB]
14	D7-D0	0	=0
15	D7-D0	0	=0
16	D7-D0	0	=0
17	D7-D0	0	=0
18	D7-D0	0	=0
19	D7-D0	0	=0
20	D7-D0	0	=0
21	D7-D0	0	=0

22	D7-D0	0	=0
23	D7-D0	0-255	Fine Gain & Normalizer LSB[1]
24	D7-D0	0-63	Fine Gain & Normalizer MSB[1]
25	D7-D0	0-255	Preset Counts LSB
26	D7-D0	0-255	Preset Counts byte 2
27	D7-D0	0-255	Preset Counts byte 3
28	D7-D0	0-255	Preset Counts MSB [Preset counts=0x0000 if unused]
29	D7-D0	0	=0
30	D7-D0	0	=0
31	D7-D0	0	=0
32	D7-D0	0-255	SCA1 Lower Threshold LSB
33	D7-D0	0-31	SCA1 Lower Threshold MSB
34	D7-D0	0-255	SCA1 Upper Threshold LSB
35	D7	0	SCA1 disabled
		1	SCA1 enabled
	D6-D0	0-31	SCA1 Upper Threshold MSB
36	D7-D0	0-255	SCA2 Lower Threshold LSB
37	D7-D0	0-31	SCA2 Lower Threshold MSB
38	D7-D0	0-255	SCA2 Upper Threshold LSB
39	D7	0	SCA2 disabled
		1	SCA2 enabled
	D6-D0	0-31	SCA2 Upper Threshold MSB
40	D7-D0	0-255	SCA3 Lower Threshold LSB
41	D7-D0	0-31	SCA3 Lower Threshold MSB
42	D7-D0	0-255	SCA3 Upper Threshold LSB
43	D7	0	SCA3 disabled
		1	SCA3 enabled
	D6-D0	0-31	SCA3 Upper Threshold MSB
44	D7-D0	0-255	SCA4 Lower Threshold LSB

[1] 'Fine Gain & Normalizer' setting controls both digital fine gain, and normalizes for different peaking times. The setting is 14 bits in size, and is:

Setting= INT[(FineGain x 8192)/PeakingTime], where

FineGain is in the range 0.75…1.25

PeakingTime is an integer in the range 1…8 (see configuration byte 6 and Table 1)

45	D7-D0	0-31	SCA4 Lower Threshold MSB
46	D7-D0	0-255	SCA4 Upper Threshold LSB
47	D7	0	SCA4 disabled
		1	SCA4 enabled
	D6-D0	0-31	SCA4 Upper Threshold MSB
48	D7-D0	0-255	SCA5 Lower Threshold LSB
49	D7-D0	0-31	SCA5 Lower Threshold MSB
50	D7-D0	0-255	SCA5 Upper Threshold LSB
51	D7	0	SCA5 disabled
		1	SCA5 enabled
	D6-D0	0-31	SCA5 Upper Threshold MSB
52	D7-D0	0-255	SCA6 Lower Threshold LSB
53	D7-D0	0-31	SCA6 Lower Threshold MSB
54	D7-D0	0-255	SCA6 Upper Threshold LSB
55	D7	0	SCA6 disabled
		1	SCA6 enabled
	D6-D0	0-31	SCA6 Upper Threshold MSB
56	D7-D0	0-255	SCA7 Lower Threshold LSB
57	D7-D0	0-31	SCA7 Lower Threshold MSB
58	D7-D0	0-255	SCA7 Upper Threshold LSB
59	D7	0	SCA7 disabled
		1	SCA7 enabled
	D6-D0	0-31	SCA7 Upper Threshold MSB
60	D7-D0	0-255	SCA8 Lower Threshold LSB
61	D7-D0	0-31	SCA8 Lower Threshold MSB
62	D7-D0	0-255	SCA8 Upper Threshold LSB
63	D7	0	SCA8 disabled
		1	SCA8 enabled
	D6-D0	0-31	SCA8 Upper Threshold MSB

5.2.3 USB Status Packet

Offset	Data bits	Allowed value	Description
0	D7-D0	0-255	Fast count LSB (Buffer A or B, depending on packet request)

1	D7-D0	0-255	Fast count byte 2 (Buffer A or B, depending on packet request))
2	D7-D0	0-255	Fast count byte 3 (Buffer A or B, depending on packet request))
3	D7-D0	0-255	Fast count MSB (Buffer A or B, depending on packet request))
4	D7-D0	0-255	Slow count LSB (Buffer A or B, depending on packet request))
5	D7-D0	0-255	Slow count byte 2 (Buffer A or B, depending on packet request))
6	D7-D0	0-255	Slow count byte 3 (Buffer A or B, depending on packet request))
7	D7-D0	0-255	Slow count MSB (Buffer A or B, depending on packet request))
8	D7-D4	3-15	FPGA version, major
	D3-D0	0-15	FPGA version, minor
9	D7-D0	0-99	Acc. Time (0-99, 1mS/count)
10	D7-D0	0-255	Acc. Time LSB, 100mS/count
11	D7-D0	0-255	Acc. Time byte 2
12	D7-D0	0-255	Acc. Time MSB
13	D7-D3	3-15	Firmware version, major
	D3-D0	0-15	Firmware version, minor
14	D7-D0	0-255	Serial Number LSB
15	D7-D0	0-255	Serial Number byte 2
16	D7-D0	0-255	Serial Number byte 3
17	D7-D0	0-255	Serial Number MSB
18	D7-D0	0	0 (N/A)
19	D7-D0	0	0 (N/A)
20	D7-D0	0	0 (N/A)
21	D7-D0	0	0 (N/A)
22	D7-D0	-128…+127	Board temp (1 degree/count, signed)
23	D7	0	DP4 detected
	D6	0	N/A
	D5	0	MCA disabled
		1	MCA enabled
	D4-D2	0	N/A
	D1	0	DP4 is unconfigured
		1	DP4 is configured

	D0	0	N/A
24	D7-D0	0-255	General Purpose Counter LSB
25	D7-D0	0-255	G. P. Counter byte 2
26	D7-D0	0-255	G. P. Counter byte 3
27	D7-D0	0-255	G. P. Counter MSB
28-63	D7-D0	0	N/A (Currently unused)

6 USE OF THE DP4 WITH AMPTEK'S XR100 DETECTORS

Amptek's DP4 Digital Pulse Processor is easily configured for use with Amptek's family of XR-100 detectors and preamplifiers. The DP4 generally comes configured for use with reset type preamplifiers, which are used in the XR-100CR for Si-PIN. This section is intended to guide a user through the set-up of the DP4 for use with these detectors. Configuration of the DP4 for other preamplifiers is described in section 0.

Some users may already have a PX2 and may be transitioning to the DP4. They can use the PX2 for initial set-up and as a power supply. Section 6.1 describes set-up and configuration for users with a PX2. Other users may not have a PX2 so will set up the DP4 directly. Section 6.2 describes set-up and configuration for users who do not have a PX2. Section X.X describes setup of the DP4 with the PC4-3 power board and the PA-210 peamplifier.

6.1 USERS WITH A STANDARD XR100 AND PX2

6.1.1 Set-up

1) Set up the PX2 and XR-100 without the DP4. This set-up is described in the PX2 manual, with a block diagram and photograph shown in Figure 8.

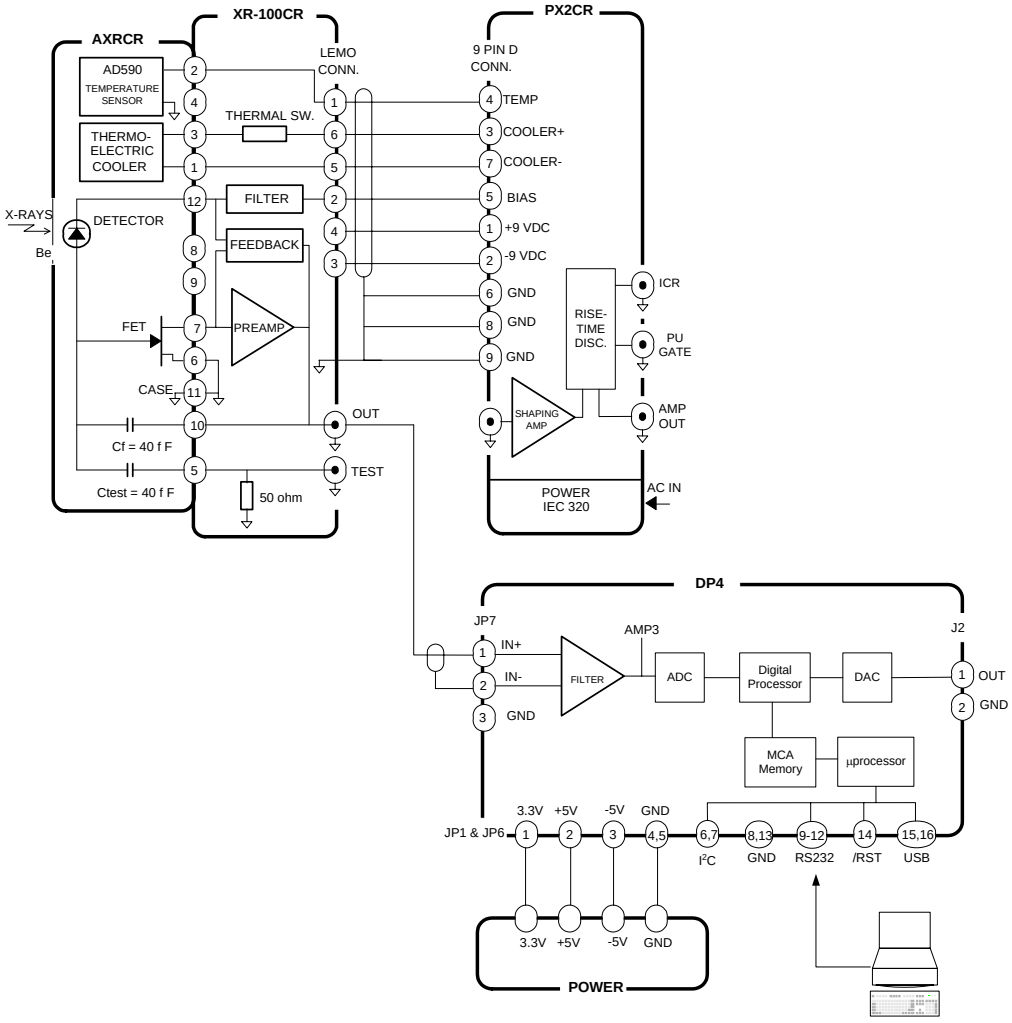
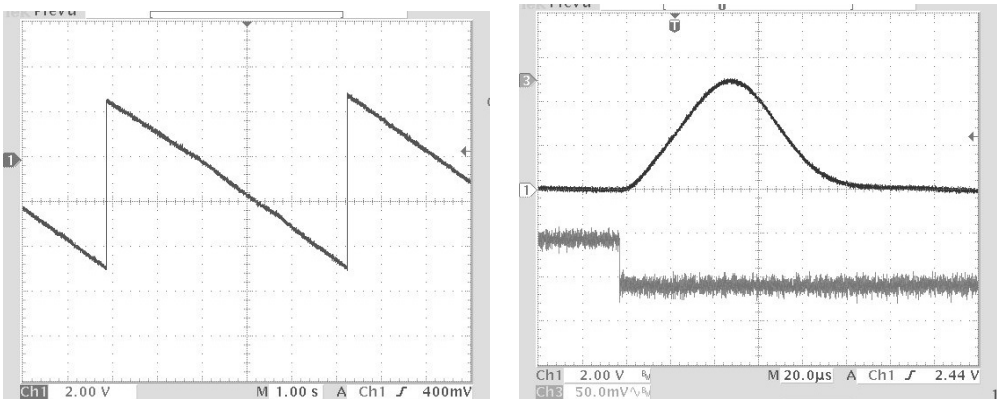


Figure 8. Block diagram of a set-up using both the PX2 and a DP4.

2) Connect the XR-100 output to an oscilloscope (using a BNC tee so it is also connected to the PX2 input) and also connect the PX2 output to an oscilloscope. Initially, set the voltage scales to 2 V/div, DC coupled, and the time scale to 100 msec/div or greater.

6.1.2 Check Out

1) Turn on the PX2. After a few seconds, the oscilloscope should look as shown in Figure 9(a). The XR100 output will have a saw tooth pattern of amplitude about 5V and a period of on the order of a second. This is due to the preamp resets. Place a source in front of the detector and the period of the saw tooth will decrease. Next set the time scale to 10 μsec/div. Now the oscilloscope should look as shown in Figure 9(b). This is the shaped pulse from the PX2. If you have an analog MCA, it might be useful to obtain a spectrum. These checks are to verify that the detector, preamplifier, and power supply are functioning properly.



(a) (b)

Figure 9. Oscilloscope traces illustrating the normal operation of the XR100 and PX2. (a) This shows the output of the preamplifier, which is input to the PX2 and DP4. The saw tooth shape is due to the reset signals. Note the scales, 2 V/div, 1 sec/div. (b) This shows the preamplifier output (bottom trace) and shaped output of the PX2 (top trace), both due to an X-ray. Note the scales. The preamplifier signal is a few mV step, which is superimposed on the several volt saw tooth shown in (a). The PX2 output is a few volts in amplitude, with a time scale of tens of μsec.

Note: When measuring signals with an oscilloscope, it is common for users to first notice the reset (because it is so large) and to confuse this with an X-ray signal. A typical X-ray interaction generates, at the preamp output, a step of a few millivolts (negative), while the reset generates a step of many volts (positive) a few times a second. The shaping amplifier inverts the signal and applies considerable gain, leading to the shaped pulse. The reset pulse is then negative going and saturates. It is important to distinguish between the two.

2) Turn the PX2 off. Now connect the DP4 and PX2, as shown in Figure 8. DP4 hardware connections are described in section 2.1. Note that the XR100 output is connected to both the DP4 and PX2, using a BNC tee. The critical connections are:

- Power: The XR100 is powered from the PX2. The DP4 requires +3.3V and +/-5V.
- Serial: The RS232 or USB connection from the DP4 to the computer is needed.
- Signal: The preamplifier output is connected to the DP4 input, JP7. Configure this connector so that the BNC shield is connected to pin 1 while the BNC signal is connected to pin 2. These are differential inputs, so pin 1 is not the DP4 ground. It is vital that a separate ground connection must be made from the XR100 to the DP4. Pin 3 of JP7 can be used. *Note:* Many users have found excessive noise because this ground connection was not made.
- Output: For debugging purposes, it is convenient to connect an oscilloscope to the DAC output at J2. Pin 2 is ground, pin 1 is signal. This is not necessary for data acquisition but helps initial set-up.

3) Start the DP4 software, as described in section 3. Figure 10 below shows a typical screen, illustrating recommended default software configurations for Amptek's XR100 detectors. These may be adjusted by the user but provide reasonable initial values. Turn on the power to the PX2, then to the DP4, then press the "Configure" button on the DP4 software.

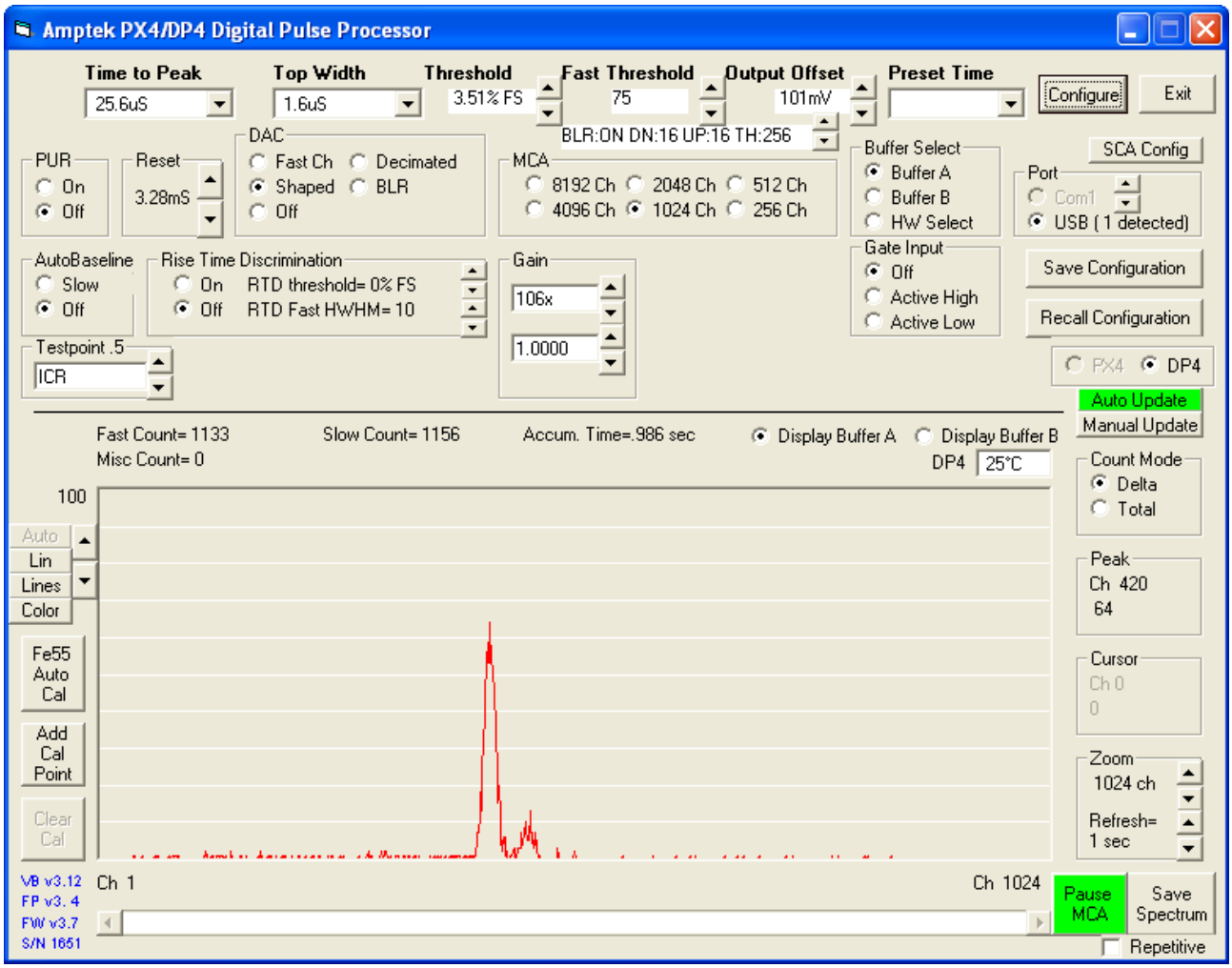


Figure 10. Screen from DP4 demonstration software, showing recommended default values for the software configuration. The peaking time, fast threshold, and slow thresholds are all very important.

4) Using an oscilloscope probe, measure the signal at the test point labeled AMP3. It should look like the trace in Figure 11. This is the input to the ADC, prior to the shaping. It is critical that this have (1) a DC offset of about 200 mV, only going negative during resets, (2) a maximum amplitude of about 1 V per pulse, and (3) a fall time of 3.2 usec.

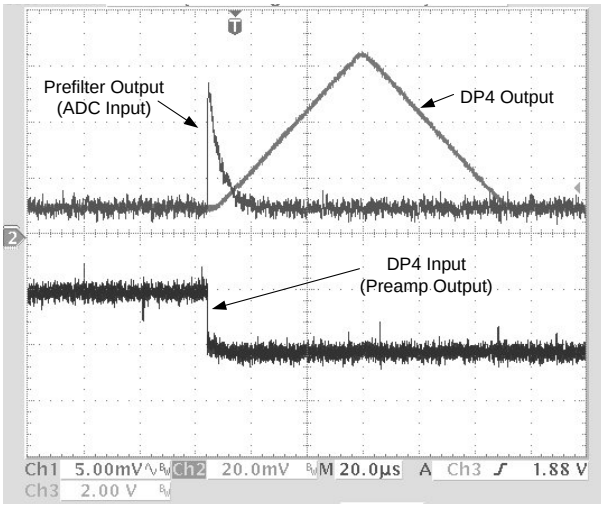


Figure 11. Oscilloscope traces obtained on the DP4, illustrating normal operation. The "prefilter output" is measured at the AMP3 test point.

5) Use the oscilloscope to compare the DP4 shaped output (J2) with the PX2 shaped output. The two traces are shown in Figure 11.

6) Check the spectrum on the DP4, to see that it matches what is expected for the source and geometry. If the signals at AMP3 and J2 are correct but no spectrum is observed, then check the software configuration.

6.2 USERS WITH A STANDARD XR100 WITHOUT A PX2

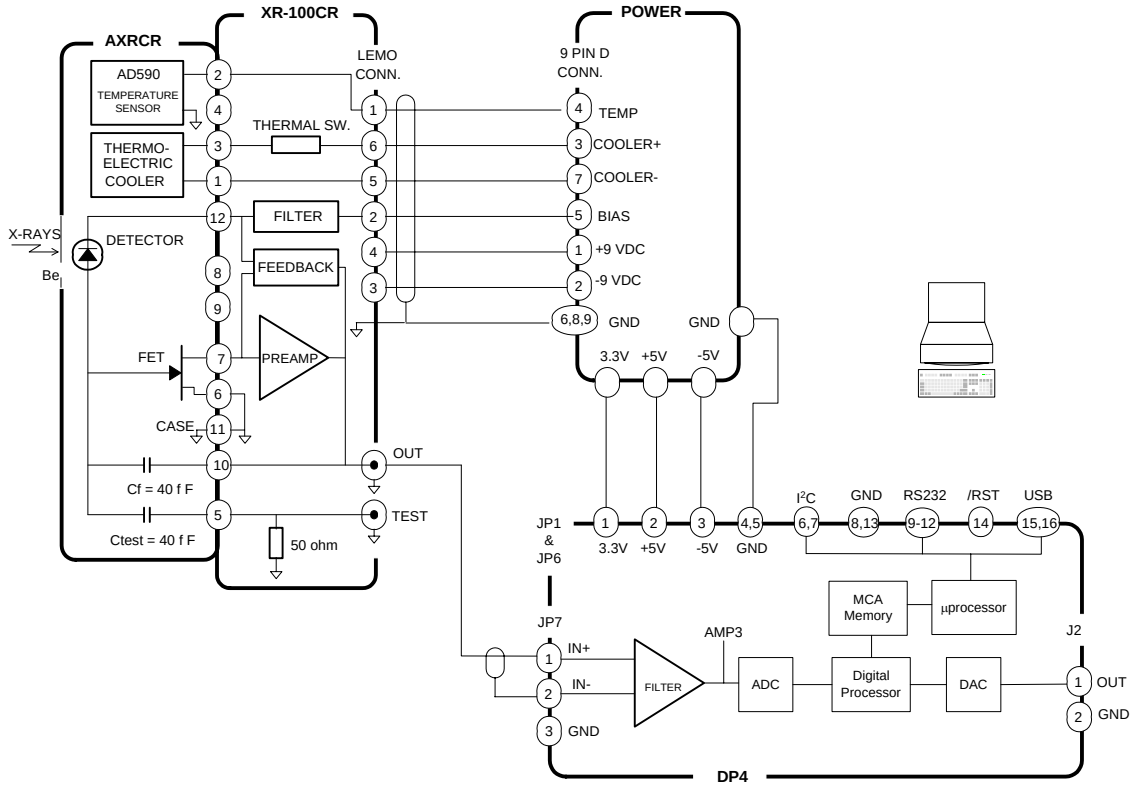


Figure 12. Block diagram of an XR100, DP4, and power supply with no PX2.

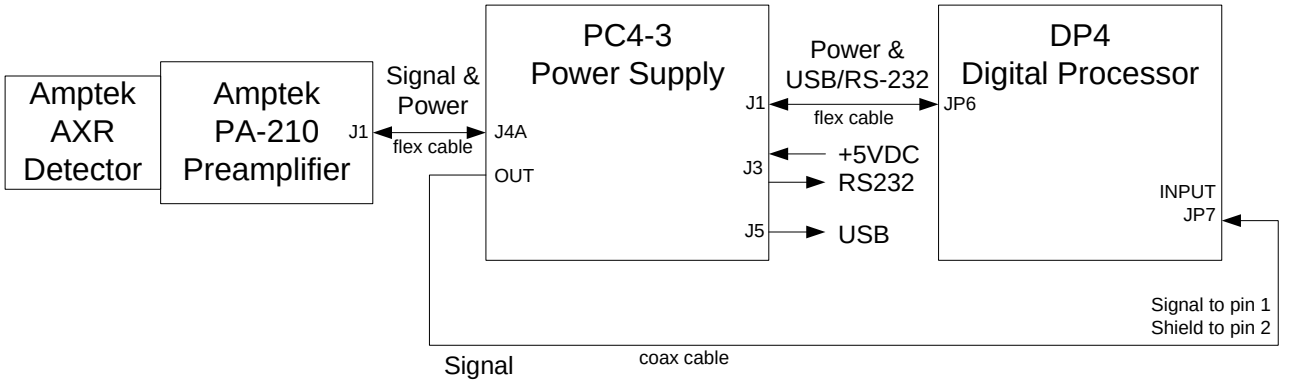
A PX2 is not required, but in its place suitable power supplies must be used. The hardware should be connected as shown in Figure 12. The power supply requirements for the DP4 are given in section 2.2.2. See the XR100/PX2 Manual (section 10 and 11) for specifications on the XR100 power requirements and appropriate setup.

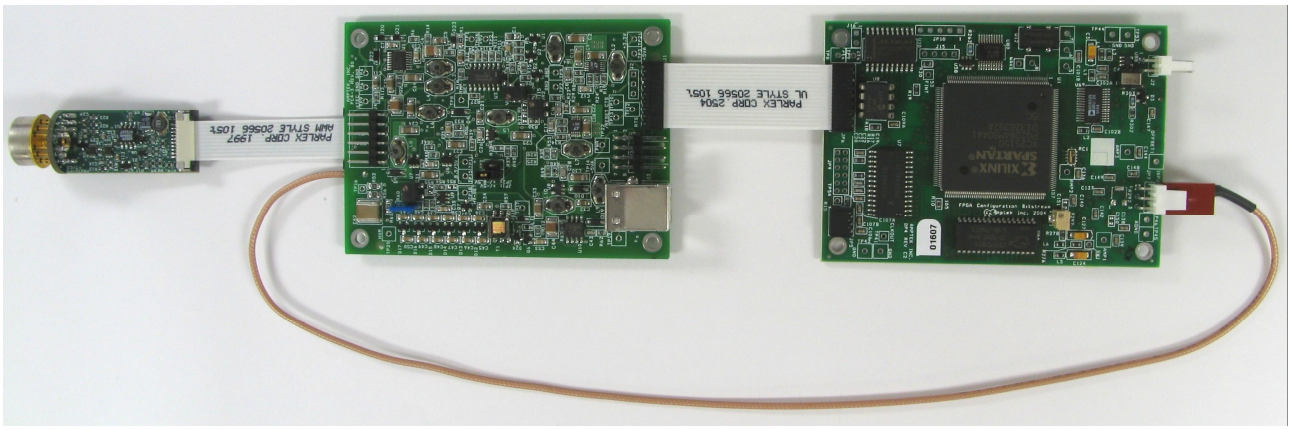
1) Make all the connections above and connect the preamplifier output to an oscilloscope. Apply power to the preamp and detector (+/-8V, bias, cooler). Monitor the temperature to verify that the detector is cooing (See XR100CR manual for details).

2) The check-out of the system should proceed as described in section 6.1.2 above.

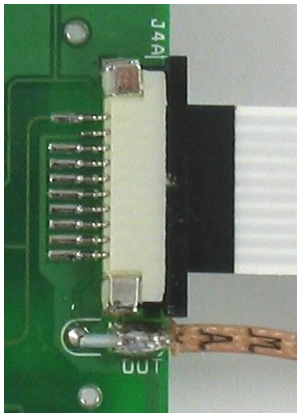
6.3 USERS WITH A DP4, PC4-3, AND PA-210 PREAMPLIFIER

Many OEMs use the DP4 together with the PC4-3 power supply board and the PA-210 preamplifier. This total OEM solution is configured as shown below.





The picture to the right is a close up of the J4A connector, which connects between the PC4-3 and the PA-210, and the OUT connection, which connects with a coax cable to the DP4 input (J7: signal pin 1, shield pin 2).



Use of the DP4 with Tail Pulse Preamps

The DP4 is configured at the factory for particular preamplifier properties, specifically for reset type feedback, for negative input signals of tens of mV, etc. It can readily be used with other preamplifiers, but this requires hardware reconfiguration. This section will guide the user in making these changes.

As shown in Figure 1, the DP4 contains an analog prefilter circuit. The output of this analog prefilter, which is the input to the ADC and can be measured a test point marked AMP3 on the DP4 board, is shown in Figure 13 as the *Prefilter Output*. The key to adapting the DP4 for various preamps is modifying the prefilter to generate the *Prefilter Output* pulse shape shown in Figure 13. If the signal measured at AMP3 has the proper characteristics, the DP4 will operate properly. This section provides suggestions regarding how the analog prefilter should be adapted for a few common situations, but it cannot cover all possibilities. In any and all cases, measuring the signal at AMP3 will allow the user to determine if the hardware has been properly configured.

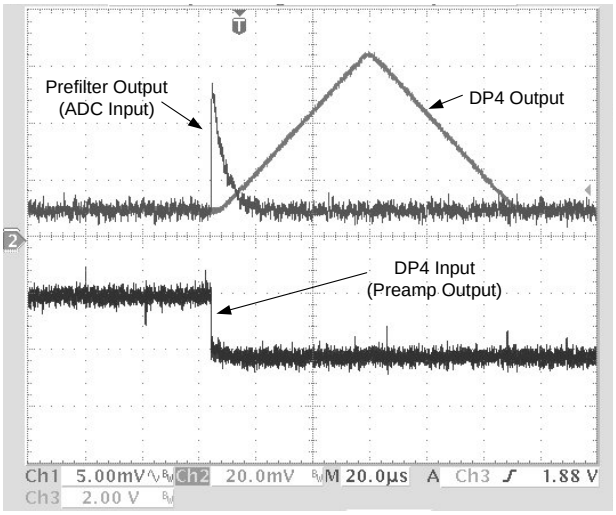


Figure 13. Oscilloscope trace showing the proper signal at AMP3.

The important characteristics of the signal at AMP3 , the output of the analog prefilter, are:

- Rise time should be >100 nsec but much faster than the peaking time to be set in the DP4 software
- The decay time must be 3.2 μsec and must be a simple, single pole decay
- The DC offset should be sufficient to keep the ADC input positive. Typically, 200 mV is good. The ADC has a range of 0 to 2V, so if AMP3 drops below 0 V, signal processing anomalies will occur. The DC offset may be increased if necessary. [AMP3 should only drop below 0V during detector reset.]
- The amplitude of the pulse must be about 1V, positive going. The ADC has a range of 0 to 2V, so if AMP3 exceeds 2V, signal processing anomalies will occur.

6.4 ANALOG PREFILTER CIRCUIT DESCRIPTION

THIS ENTIRE SECTION MUST BE REDONE FOR NEW REFERENCE DESIGNATORS

The analog prefilter circuit is shown in Figure 14. The main elements are (1) a differential amplifier (U83), (2) a high pass filter with a 3.2 μsec time constant, (3) a gain stage (U86), and (4) an amplifier (U82B) providing gain, polarity reversal, and DC offset adjustment. We will now discuss these in more detail.

6.4.1 Differential amplifier

This is a (nominally) unity gain differential amplifier, used to reduce common mode ripple. This circuit also permits the user to invert the signal: the output of the differential amplifier should be a negative going pulse, so the preamp signal can be connected to either the inverting or noninverting node of the differential amplifier. This circuit can also provide some gain or attenuation, using the input resistors.

Note that this signal return is connected to the differential amplifier input and not to DP4 ground. The signal reference does not provide a ground connection. The preamplifier ground must be connected directly to the DP4 ground. Pin 3 of JP7 may be used or some other ground point. Failure to ground the preamp, connecting the preamp ground only to the differential amplifier input, has caused many users significant grounding problems!

6.4.2 High Pass Filter

(R297 + R300) together with C133 form a high pass filter, which provides the 3.2 μsec decay seen in the Prefilter Output in Figure 13. Pot R297 is used to fine-tune the time constant. If this pole is set correctly, then the shaped trapezoidal output from the DP4 DAC will have a flat top and a clean tail (no undershoot or overshoot). Setting this pole is very important to the proper operation of the digital pulse processor.

If a preamplifier with a tail is used, i.e. one using resistive feedback, then there will be an undershoot at the output of this filter. This can be seen at AMP2, AMP3, and at the DAC's shaped output. A pole zero resistor must be installed in R292 to cancel the preamp tail. The procedure for doing this is contained in section 6.5.1.

The switch U84 may be used to measure the DC offset which is input to this circuit. This is commonly used with reset-type preamplifiers, which do not need baseline restoration.

6.4.3 First Gain Stage

The first gain stage, based on U86, can provide a gain of either 5 or 10. The gain is changed by switch U85A, under command from the microprocessor. Note that any DC output from the high pass filter is amplified by this gain.

6.4.4 Final Gain Stage

The final gain stage, U82B, implements several important functions:

1) It provides additional coarse gain, of approximately 2 or 10, by switch U85A.

2) IIt inverts the signal. The pulse measured at AMP3 must be positive going.

3) It provides a DC offset, by pot R287. The offset input to this amplifier stage ranges from -100 to +100 mV. The pulse measured at AMP3 must have a DC offset sufficient to ensure that the ADC input does not go negative.

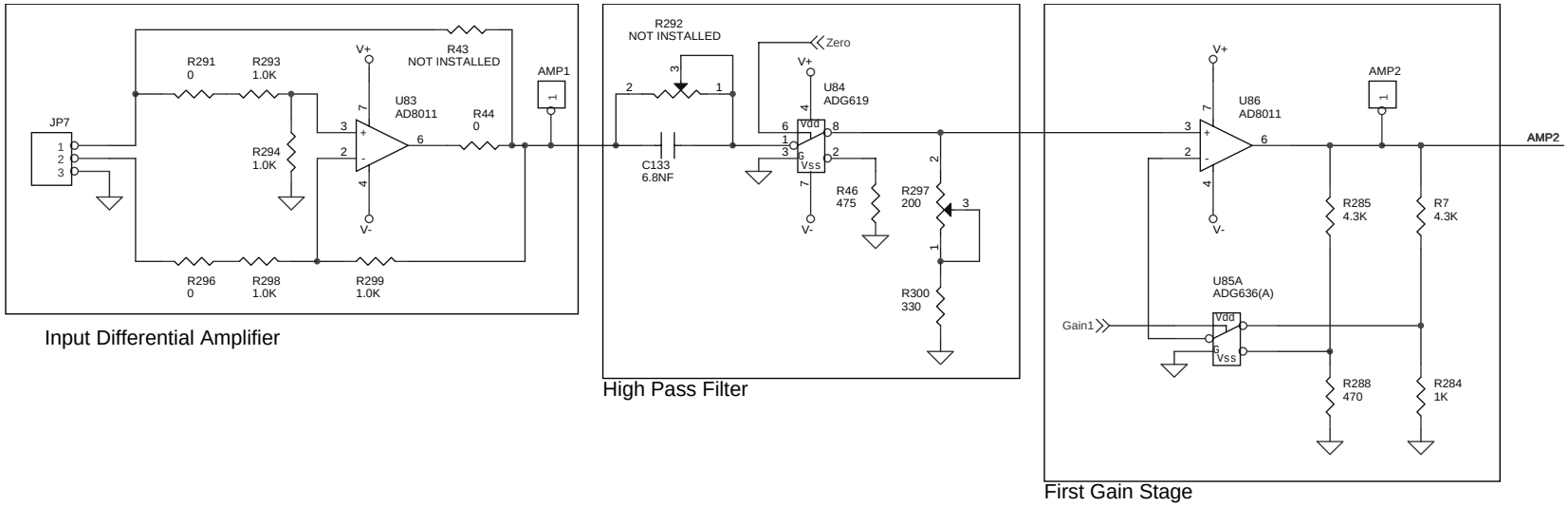


Figure 14. Schematic of the analog prefilter in the DP4. [Renumber]

6.5 PROCEDURES FOR COMMON CHANGES

The following sections recommend ways in which the DP4 can be modified to match the output requirements of given preamplifiers.

6.5.1 Preamplifier Tail Cancellation

The most common change required is to add a pole zero resistor to cancel the tail of a preamplifier with continuous feedback. The following procedure is suggested:

1) Estimate the value of R292. Let τ be the preamplifier time constant, the time in which the preamp tail decays to 1/e of its peak value after a step. Then R292 = τ/6.8 nF. For τ=1 msec, R292=147kΩ.

2) Install R292. It is usually best to first install a pot to accommodate tolerances in the various components. With the pot installed and set to the approximate value, turn on the system and measure at AMP3 with an oscilloscope, with signals coming through. Look for a long undershoot or overshoot, comparable to the preamp tail. Typical waveforms are shown in Figure 15. If there is an undershoot, decrease R292. If there is an overshoot, increase R292. Once the precise value is found, a fixed resistor may be installed.

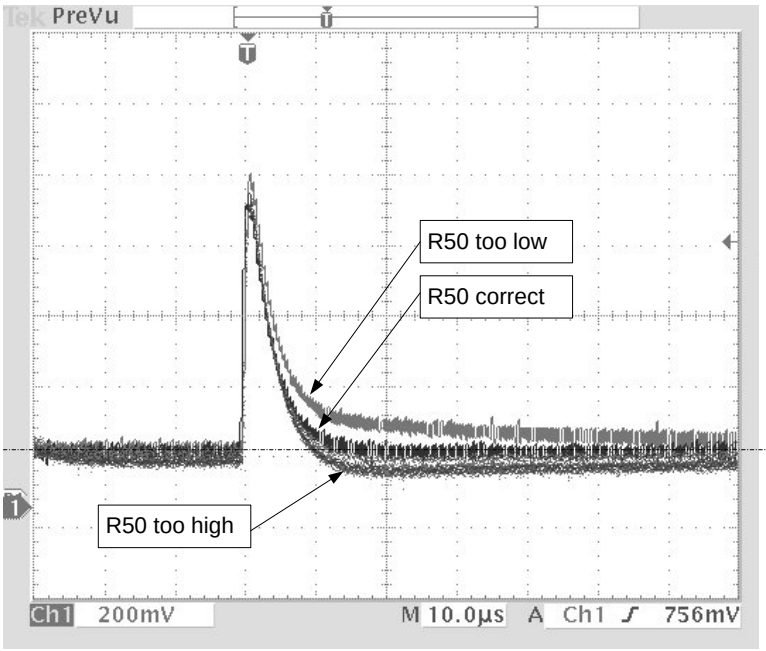


Figure 15. Oscilloscope traces showing AMP3 under several conditions. (a) R292 properly adjusted. (b) R292 too large. (c) R292 too small. When R292 is correct, there is neither undershoot nor overshoot on the tail.

3) The presence of R292 will change the time constant of the high pass filter, leading to a slope on the trapezoidal top and to an undershoot or overshoot of short time constant. Typical waveforms are shown in Figure 16. Using the DP4 DAC output, set the peaking time to a short value and the flat top duration as long as permitted. Adjust R297 until the top is flat and no undershoot or overshoot is visible.

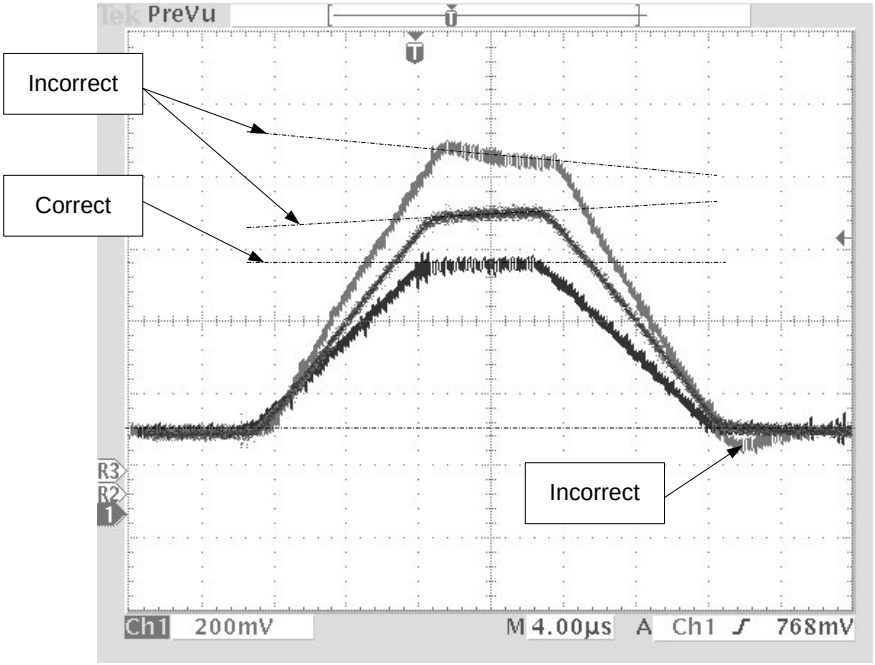


Figure 16. Oscilloscope traces showing the DAC shaped output under several conditions. (a) R297 properly adjusted. (b) R297 improperly adjusted. When R297 is incorrect, the top of the trapezoid is sloped and there is an undershoot or overshoot at the end.

4) The presence of R292 also leads to a DC offset into the circuitry. A preamp generally has some DC offset at its output, and R292 combines with (RR297+R300) to form a DC divider, coupling a fraction of this offset into the amplifiers, which is then amplified. The DC offset should be measured, first at AMP2 and then at AMP3. If the offset is small enough, then the offset adjust pot R287 can accommodate it. If the offset is a bit larger, then R51 and/or R303 can be decreased to provide more range.

5) The diode D1 is only needed to clamp the ADC input in the presence of large, negative reset pulses. We recommend removing it for non-reset preamplifiers.

This procedure will only work if the tail from the preamplifier is a simple exponential (a single pole) and is constant. If there are multiple poles in the preamplifier response, then the dominant pole may be cancelled. The remaining pole(s) may or may not affect proper operation. If the time constant varies, i.e. with temperature or count rate, then the pole will not be cancelled under all conditions.

6.5.2 Inversion

JP7 is the input connector. For positive (negative) going preamp outputs, connect the signal to pin 2 (1). The signal reference from the preamp should be connected to pin 2 (1), respectively.

6.5.3 Input Range Adjustment

U83 has a signal range of $\pm$4V. Many preamps have a larger dynamic range, i.e. their output may swing from +/- 12V. In such cases the input resistors may be used to attenuate the preamplifier signal. Change R291 and R296 (which must be equal) to provide the necessary attenuation. This will cause a slight loss of resolution so should only be used if it is really needed. Alternately, if the preamplifier signal is limited to a smaller range, then this circuit can be configured to provide a small amount of gain, using resistors R293 and R298.

6.5.4 Single Ended Operation

The DP4 is configured at the factor of a differential input, but may be reconfigured for single ended operation. Using differential input has several advantages: it reduces common mode interference (with

proper grounding) and it uses a buffer which separates the output impedance of the preamplifier from the DP4's high pass filter. However, some users prefer single ended operation. To achieve this:

1. Remove resistors R291, R296, and R44.
2. Install a zero ohm resistor in R43.

Pin 1 of JP7, the input, will now go directly to the high pass filter. Pin 2 is not used, while Pin 3 is the ground node.

7 DEAD TIME IN THE AMPTEK DP4

Many users have asked "what is the dead time in the DP4"? Often, they are used to working with MCAs which have a "live time clock" which is turned off during "conversion", the time the peak height is sampled and digitized. But the DP4 has no dead time associated with digitizing the peak amplitude. The incoming pulse stream is digitized at a high rate (20 MHz, every 50 nsec) and then filtered. The peak digital value is determined with no conversion delay (one of the advantages of digital processing). Another advantage of the digital processing arises from the triangular pulse shapes, which are symmetric and return to a true baseline after twice the peaking time. This makes the timing intervals for pile-up and pulse losses very predictable.

In most cases, the reason a user asks for the dead time is to accurately determine the true incoming count rate (ICR). Even though there is no conversion dead time in the DP4, there are counting losses in both the fast and slow channels. This section will explain these losses and how to determine the ICR from the measured rates. This ection also explains how to compute the pulse counting losses one can expect.[2]

7.1 FAST CHANNEL

The DP4 fast channel signal has a 400 nsec peaking time, and it is this peaking time which is the dead period of the fast channel. It is the rising portion, not the full width. If a second event occurs within 400 nsec of the first, then the second is not counted and a single fast count is recorded. This dead period occurs for 400 nsec after every event, whether recorded or not, so the fast channel counts are described by a paralyzable model. If the true input count rate is R_{In}, the fast channel dead time is τ_{FAST}=400 nsec. and the output count rate from the fast channel (R_{FAST}) is given by

$$R_{FAST} = R_{In} e^{-(R_{In}\tau_{FAST})} \quad [1]$$

The PX4 does not stop its clock during these dead periods. To estimate the incoming count rate, this equation cannot be used. There is no closed form solution for the true rate, given the fast rate. One can approximate this as a non-paralyzable system and obtain

$$R_{In} \cong R_{approx} = \frac{R_{FAST}}{1 - R_{FAST}\tau_{FAST}} \quad [2]$$

Figure 17 shows R_{FAST} versus R_{In} (dark line) and also the throughput, the fraction of counts which are measured by the fast channel (line with filled circles). The accuracy of the approximation in equation [2] is shown by the line with open circles. At $1x10^5$ sec^{-1}, the fast channel records 96.1% of the incoming counts. R_{approx}, the approximate correction, has an error of <0.08% at this rate. For most purposes, the fast channel count rate measurement is the best way to estimate the true incoming count rate.

[2] This discussion and the equations are based on the discussion by G.F. Knoll, *General properties of radiation detectors*, Chap 4 in **Radiation Detection and Measurement**, John Wiley & Sons, New York (1989), pp 120-122

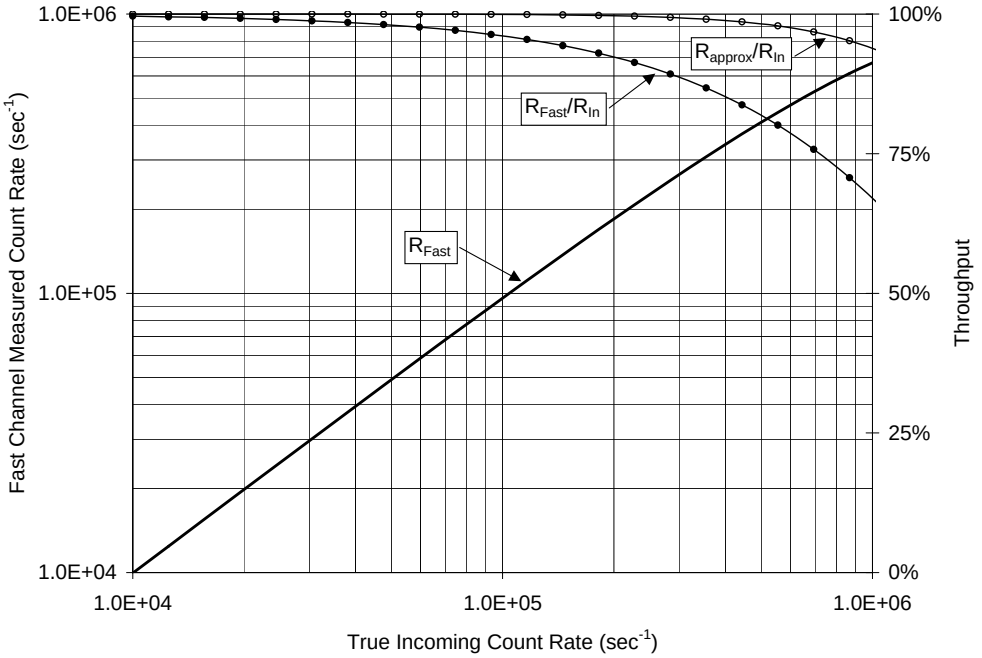


Figure 17. Plot showing the throughput of the fast channel versus input count rate.

7.2 SLOW CHANNEL

The slow channel count rate varies depending on the pile-up rejection settings. Figure 18 shows two cases. In the plot on the left, the two pulses are separated in time by more than the peaking time. They can clearly be recognized as separate pulses and accurate peak heights can be measured. Both are valid events and will be recorded in the spectrum and in the slow channel counts. Because of the symmetry of the triangular shaping, if the pulses are separated by more than the peaking time, they are not piled up. This is unlike an analog shaper, where the pulses are asymmetric.

In the plot on the right, the two pulses are separated by less than the peaking time. Only a single pulse occurs at the shaped output, with amplitude near the sum of the two. If pile-up rejection is turned off, then this is recorded as a single event with incorrect amplitude. If pile-up rejection is turned on, then both events are rejected. Nothing appears in either the slow channel counts or in the spectrum.

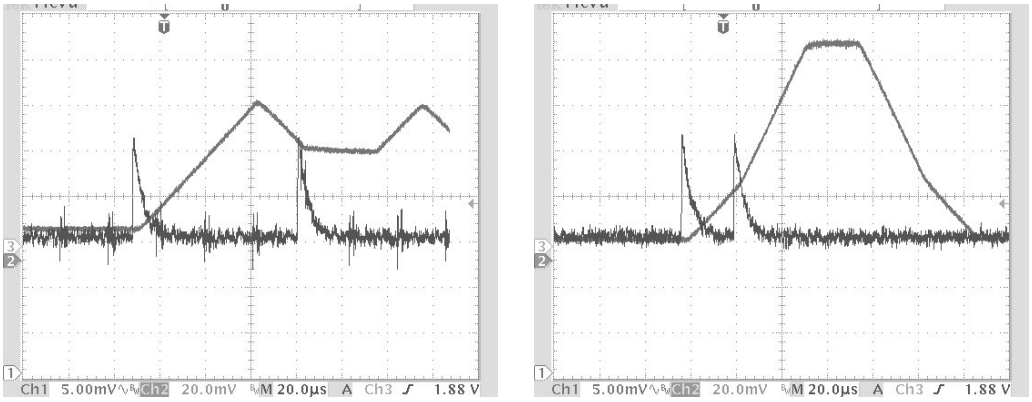


Figure 18. Oscilloscope traces showing (left) two pulses which are separately detected and accurate pulse heights measured and (right) two pulses which overlap in time. These plots show the output of the analog prefilter (the tail pulses) and the shaped output.

The window for pile-up rejection is (1 + 3/16) of the peaking time. If pile-up reject is on, this is the dead period and the equation for OCR reflects the fact that two events are removed. If pile-up reject is off, the

dead period is closer to the peaking time (plus some small jitter) and only one event is removed. The measured rates are

$$R_{PUR\_Off} = R_{In} e^{\left(-R_{In}\tau_{peak}\right)}$$
$$R_{PUR\_On} = R_{In} e^{\left(-2R_{In}(19/16)\tau_{peak}\right)} \quad [3]$$

Figure 19 shows computed (lines) and measured (circles) output count rates versus input count rates, at several peaking times. The computations use the formula in equation [3]. Excellent agreement is clearly seen between measurement and calculations.

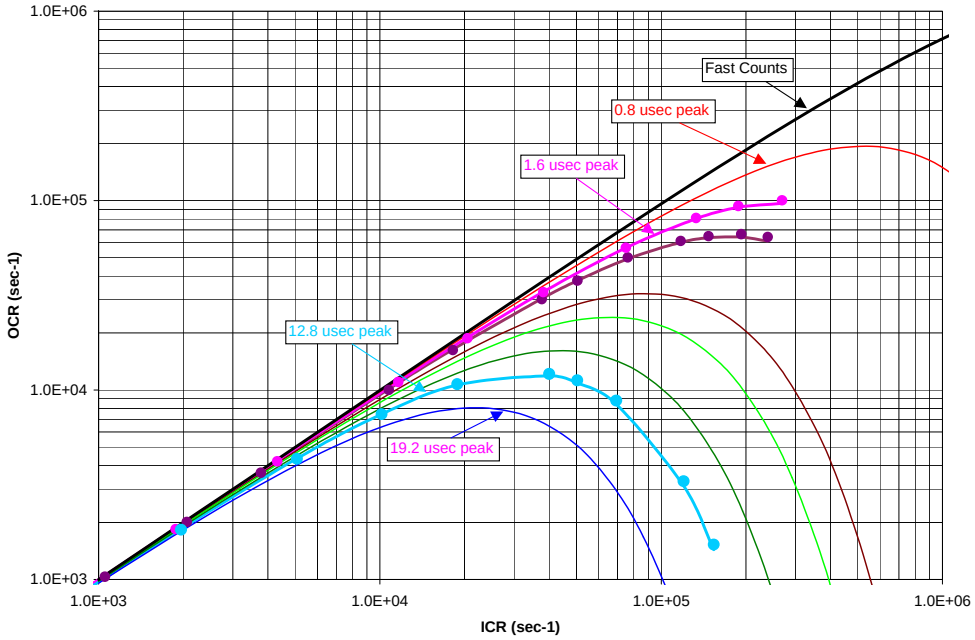


Figure 19. Plot showing measured and computed input and output count rates, with pile-up rejection on, for various peaking times.

7.3 ACQUISITION TIME

The DP4 provides the fast counts, the slow counts, and the "acquisition time". It is important to define this acquisition time. This is the real elapsed time during which data are being acquired. The real time clock is turned off during certain events, including data transfers over the serial bus and also including reset intervals. If a reset preamplifier is used, and the DP4 is configured for a certain reset time period, then acquisition is shut down during the reset period and the acquisition clock is stopped. This acquisition time is measured using a typical 20 ppm crystal oscillator so is quite accurate. The true count rate should be computed using the actual acquisition time rather than the nominal data transfer time.

Data transfers occur based on an approximate real time clock. For example, one might configure the DP4 to update every second. When the data transfer occurs, the acquisition time is shown and this will probably differ from the nominal "1 second", due to the approximate clock and also due to reset losses. A typical value is 1.05 second. At high count rates, a reset preamp resets more often, and so there is less acquisition time per transfer. In this case, the acquisition time might become 0.85 seconds. On the screen, this time is displayed along with the fast counts and the slow counts during the same interval. The actual count rate is found by dividing the observed counts by the observed acquisition time, 0.85 seconds for this example.

7.4 TIMING SUMMARY

In the following, the pulse separation time is denoted T.

1) $T > (19/16)\tau_{peak}$: Both are recorded in the spectrum with correct amplitude, and both are recorded in both fast and slow counts. True for PUR on and off.

2) $(19/16)\tau_{peak} > T > 400$ nsec: With PUR on, neither is recorded in the spectrum or in slow counts but both are recorded as fast counts.

3) $\tau_{peak} > T > 400$ nsec: With PUR off, a single event is recorded in the spectrum (with incorrect amplitude), a single slow count is recorded, but both are recorded as fast counts.

4) 400 nsec > T: A single event is recorded in the spectrum (with incorrect amplitude), a single slow count is recorded, and a single fast count is recorded. True for PUR on and off.

This presumes that both events are above both the fast and the slow thresholds. For signal amplitudes near threshold, one or both might not be recorded. The fast and slow thresholds are different (the fast threshold is usually higher than the slow) so an event may be recorded in one channel but not the other.

8 TROUBLE-SHOOTING GUIDE

Configuration

- If the fast threshold is too low, then noise counts will trigger the pile-up reject circuit. This can veto most or all of the actual events. This threshold can be raised or the PUR can be disabled.
- If the fast threshold is too high, then piled up events might not be rejected.
- Both pile-up rejection (PUR) and risetime discrimination (RTD) are used to select those pulses which are recorded. If the settings are wrong, the incorrect pulses are recorded and in many cases, no pulses are recorded. If no spectrum appears, the first diagnostic step should be to turn off PUR and RTD

Grounding

- Care must be taken in grounding the DP4. In particular, noise problems may occur if the signal ground that connects the preamplifier to the DP4 input is a power return.
- Amptek has observed at least one Dell laptop that injects significant current via the RS232 ground into the DP4, which seriously upsets performance. Our solution is to use a 3-prong to 2-prong AC adapter on the laptop, which disconnects the laptop power supply from AC ground.

9 INDEX

analog prefilter 3, 6, 15, 39, 40, 41
auto baseline 7, 16, 21, 24, 29
baseline restoration 7, 16, 29
gate 9, 17, 24, 29
MCA 4, 17, 23, 24
pile up rejection..... 7, 17, 21, 23, 28
preamplifier 3, 4, 6, 11, 12, 16, 20, 34, 39, 42
pulse shaping..... 3, 5, 15, 21
reset preamplifier ... 4, 6, 12, 16, 21, 23, 28, 34, 39
risetime discrimination 8, 17, 21, 24, 29
RS232 interface 19, 24
serial interface..... 4, 10, 11, 13, 19
threshold 7, 8, 17, 21, 23, 28, 48
USB interface.....19, 24

Current version as of manual release date: PCB rev C2, VB rev 3.13, FP rev 3.4, FW rev 3.8

END OF DOCUMENT

Product Documentation

Tentative

Tube N°

06-0172

X-Ray Tube

MTI-40-2-AG-500

P/N 915601.01

Documentation-No.:
DK-915601.01E

Original text: English

COMET

Revision record

Issue	*Date*	*Remarks*
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TABLE OF CONTENT

1 SCOPE 5

2 INTENDED USE / GENERAL CHARACTERISTICS 5

3 WARNINGS 5

4 TECHNICAL SPECIFICATIONS 7

5 INSTALLATION 10

6 PERIODIC MAINTENANCE 10

7 DISPOSAL 10

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1 Scope

This document is applicable to the following part:
X-ray Tube MTI-40-2-AG-500, Part number 915601.01

Definitions in this product documentation

A Note is a text that is only there for additional information.

A Caution is information indicating a danger that could damage or destroy equipment.

A Warning is information that indicates a danger that could potentially harm or kill persons.

2 Intended use / General Characteristics

The MTI is an industrial X-ray Tube in metal ceramic technology. Its intended use is in industrial applications for non destructive testing purposes. It is not to be used for medical applications.

3 Warnings

Introduction

Proper use and safe operation of X-ray tubes are the responsibility of the equipment manufacturer and user of such tubes. The manufacturer provides information on its products and associated hazards, but it assumes no responsibility for after-sale operating and safety practices. Limited life is an inherent characteristic of x-ray tubes. Take appropriate action through redundancy or other safeguards to protect personnel and property from tube failure.

The X-ray Tube emits x-ray. Please observe the local and international regulations!

Do not operate this tube except in accordance with safety-information and additional instructions provided by the original equipment manufacturer.

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COMET supplies the tube without any radiation protection. Appropriate shielding must be provided by the original equipment manufacturer in accordance to local regulations.

X-ray Tubes are operated at voltages high enough to kill persons through electrical shock. Appropriate isolation must be provided by the original equipment manufacturer.

The X-ray Tube contains Beryllium (tube window). At the end of useful life of the tube the Be-window must be disposed in accordance with your local regulations.

Fumes of Beryllium metal (or its compounds) as well as dust can be hazardous if inhaled.

During use, corrosion products may occur on the Be-window, but these should not be scraped off, machined or otherwise removed.

The X-ray Tube is not to be operated in air. Appropriate isolation must be provided by the original equipment manufacturer.

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4 Technical specifications

Tube Voltage	10 ... 40 kV
Tube Current	0 ... 50 µA
Continuous Tube Power	max. 2 W
X-ray window	Be
X-ray window thickness	0.5 mm
Target Material	Ag
Radiation angle	> 100°
Filament voltage	max. 1.3 V
Filament current	max. 1.0 A
Anode temperature	max. 100°C
Mounting orientation	any

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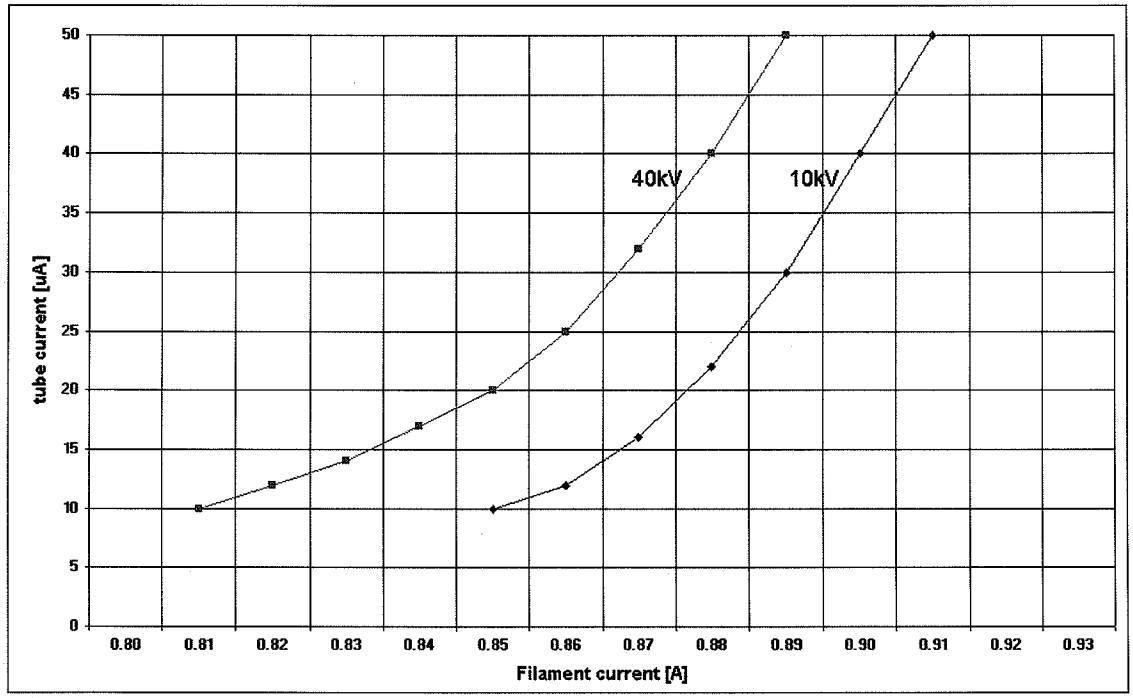
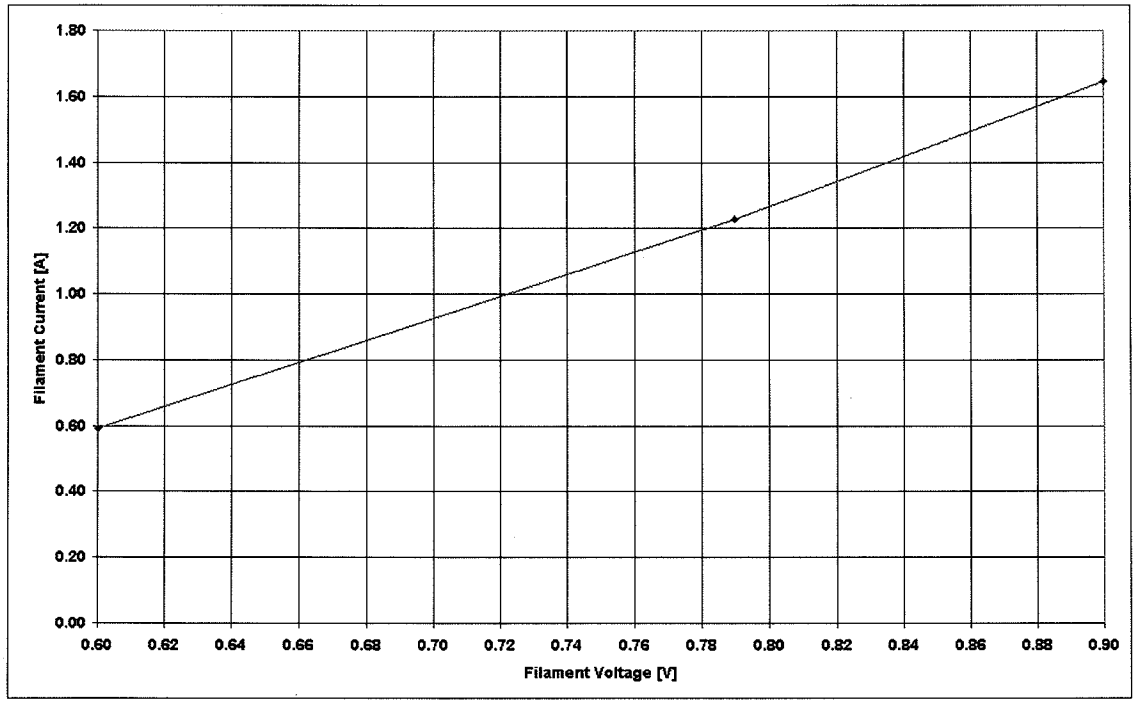
Tube emission characteristics (typical)



Filament characteristics (typical)



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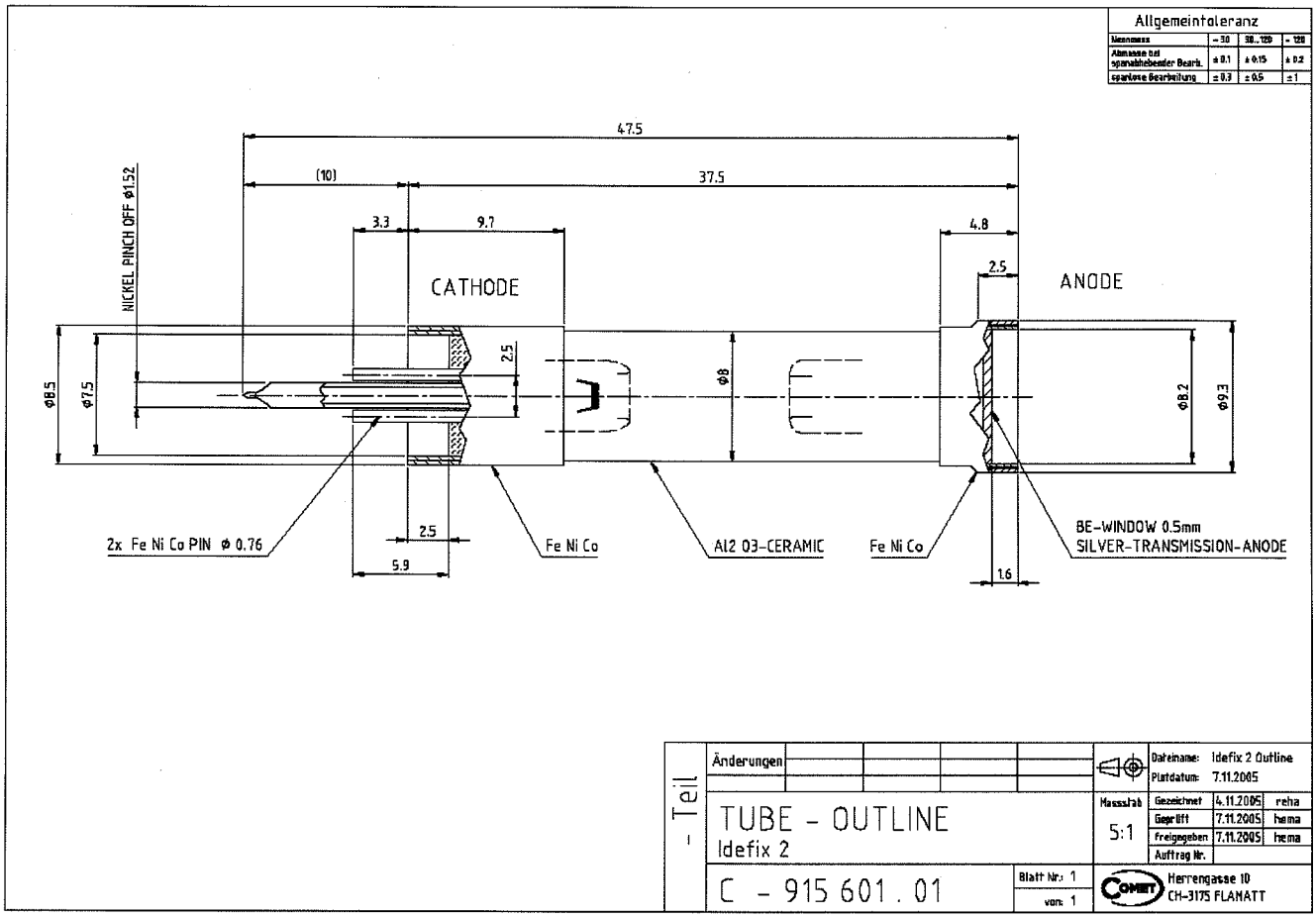
Mechanical Dimensions:



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5 Installation

The tube is shipped to the customer in a single package ready for assembly.

Warning

Before starting the assembly, take into account the following precautions to avoid personal injuries:

- **Read the operation manual**

Caution

The X-ray tube may only be installed by trained personnel.

6 Periodic maintenance

No periodic maintenance is required.

7 Disposal

Warning

The X-ray tube contains Beryllium (tube window). At the end of useful life of the tube the Be-window must be disposed in accordance with your local regulations.

Fumes of Beryllium metal (or its compounds) as well as dust can be hazardous if inhaled.

During use, corrosion products may occur on the Be-window, but these should not be scraped off, machined or otherwise removed.

Apart from that, this product contains no dangerous parts and can be disposed of as standard electrical waste; the metal parts can be treated as standard metal waste.

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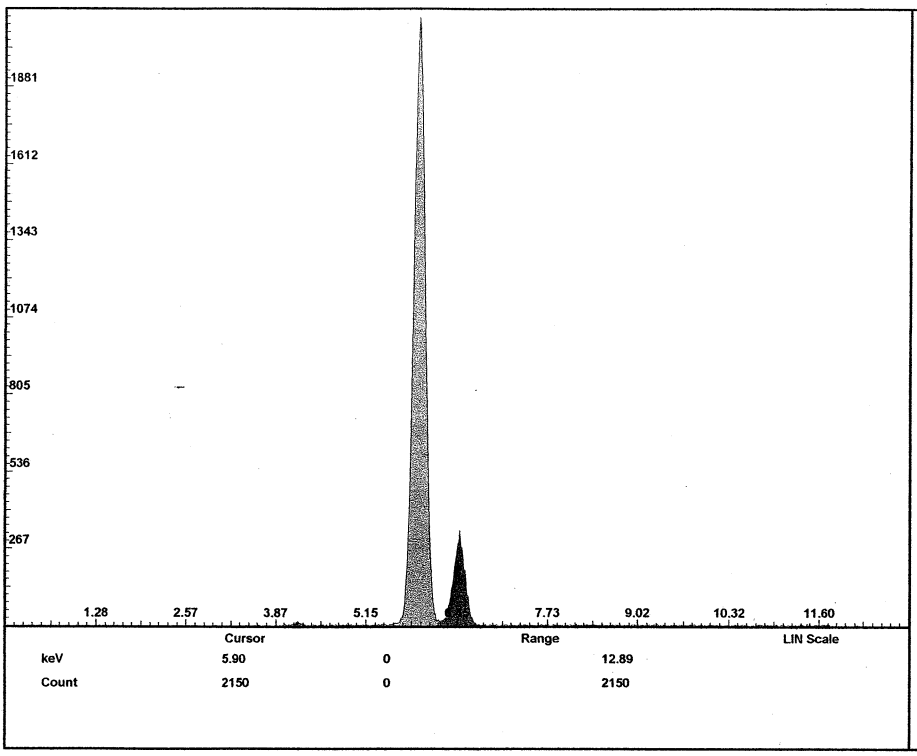
Z:\SPECTRA FOLDER\XR100cr-6mm2-500uM Spectra\AXR31038_6mm2_500uM_12.8uS_Fe55_University of Washington.mcaFe55 05/19/2006 08:37:53

University of Washington



DP4 (s/n 1811)
Tag:
Fe55

Mode	MCA
Channels	1024
LLD Thresh	6.15% FS
Fast Thresh	20
Peak Time	19.2uS
Gain	106.00
Gain Delta	
Preset Mode	None
Preset	0
Real Time	25.44
Counts	39790
Input Counts	11612835
Total Rate	456515.25
Dead Time	99.66%

Start Time:
05/19/2006 08:37:53
Status:
disconnected

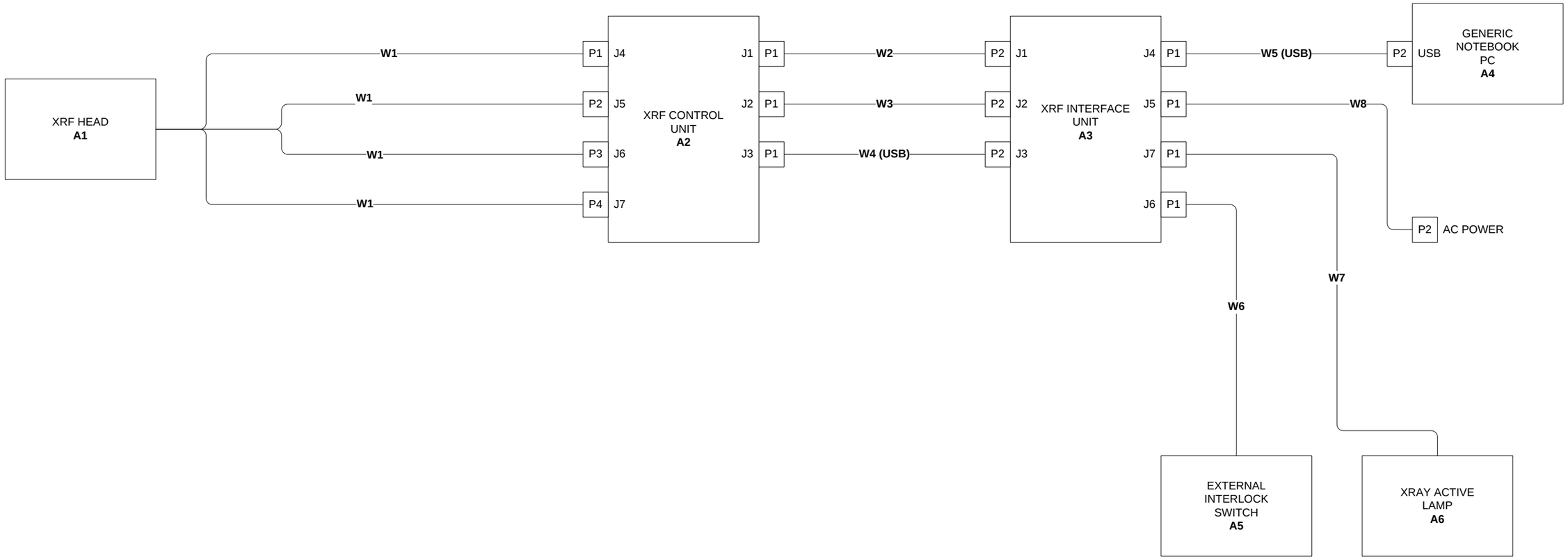
Peak Information:

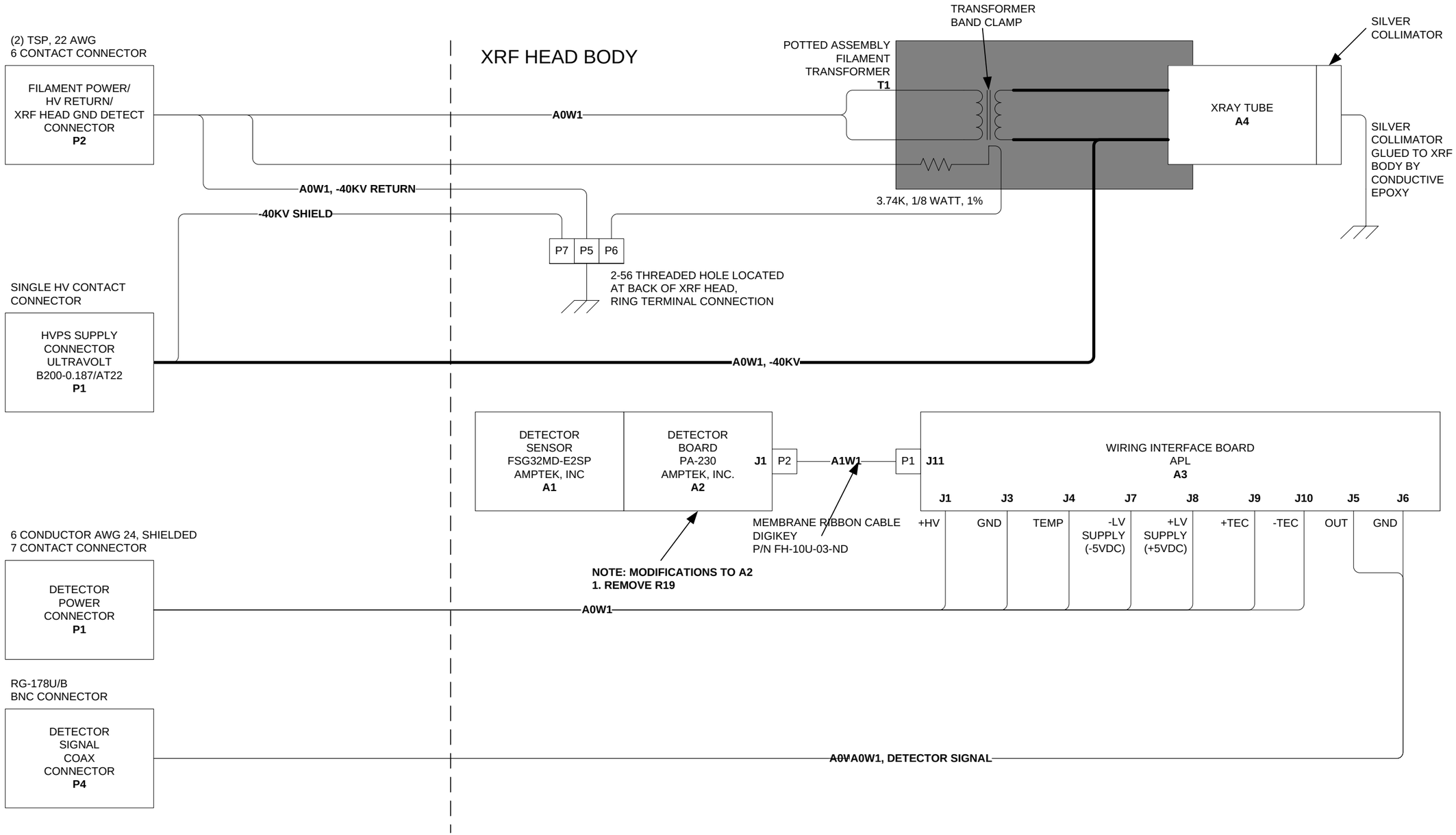
Centroid (N)	5.90
FWHM (N)	0.180
Net Area	32711
Uncertainty	0.56
Net Rate	1285.89
Gross Area	33229

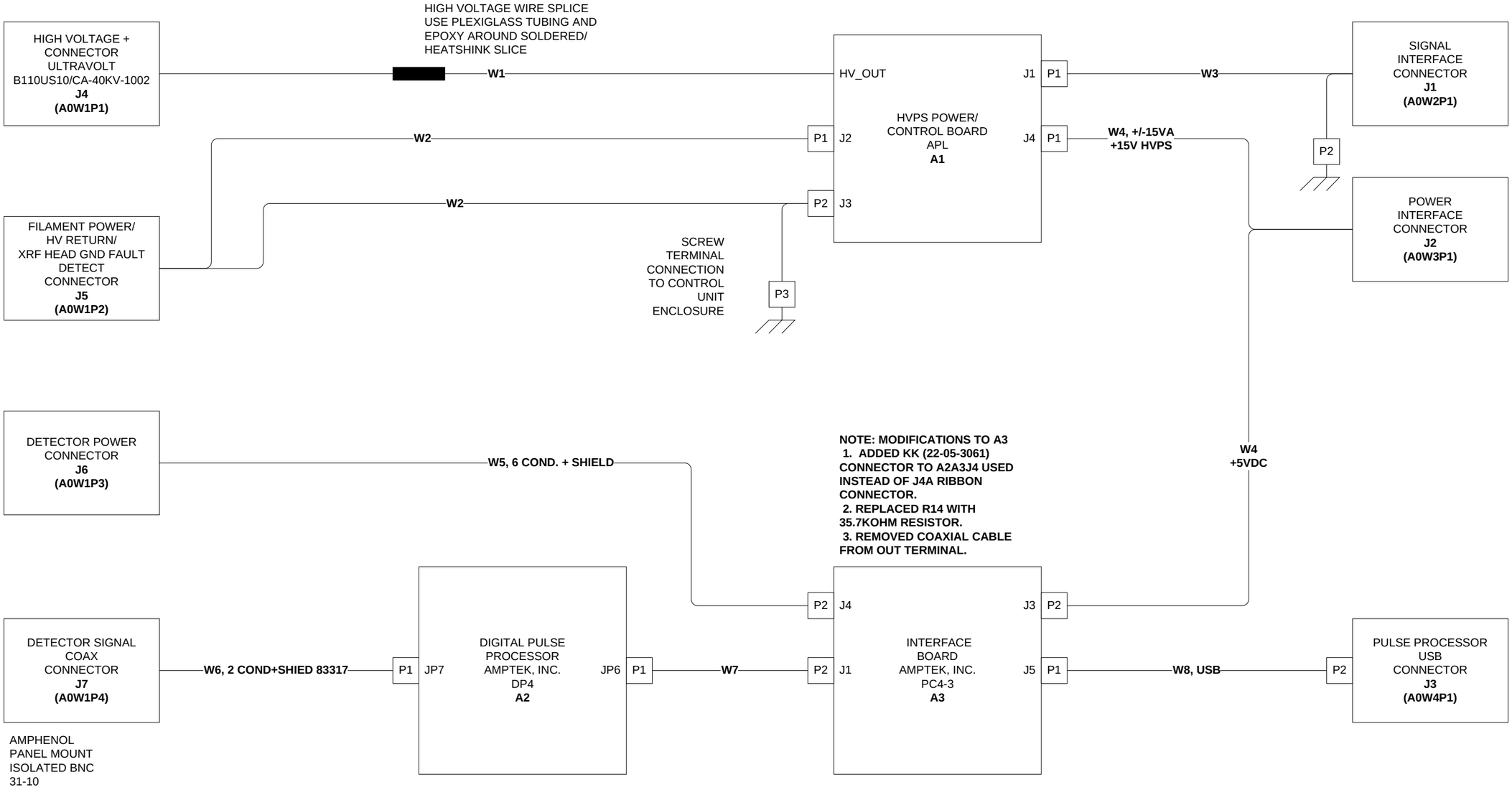
Board Temp 27°C

AXRCR S/N: 31038 DP4 S/N: 1811
Be Window Thickness - 0.5 mil, Temperature Sensor - Diode, Collimator - Internal Multilayer,
Cooler Stage - 2 stage, Detector Thickness - 500uM, Detector Area - 6mm2, Detector Type - Silicon,
Feedback Type - CRF, Assembly Type - Part Only
T = 758mV, FWHM@5.9keV: 180eV, Tested with 12.8uS Peak Time, HV Bias: 160 Volts, Cooler Current: 350mA,
Amptek Code # AR-FSG32MD-E2SP, Preamp SN: D01938
Fe55 Configuration

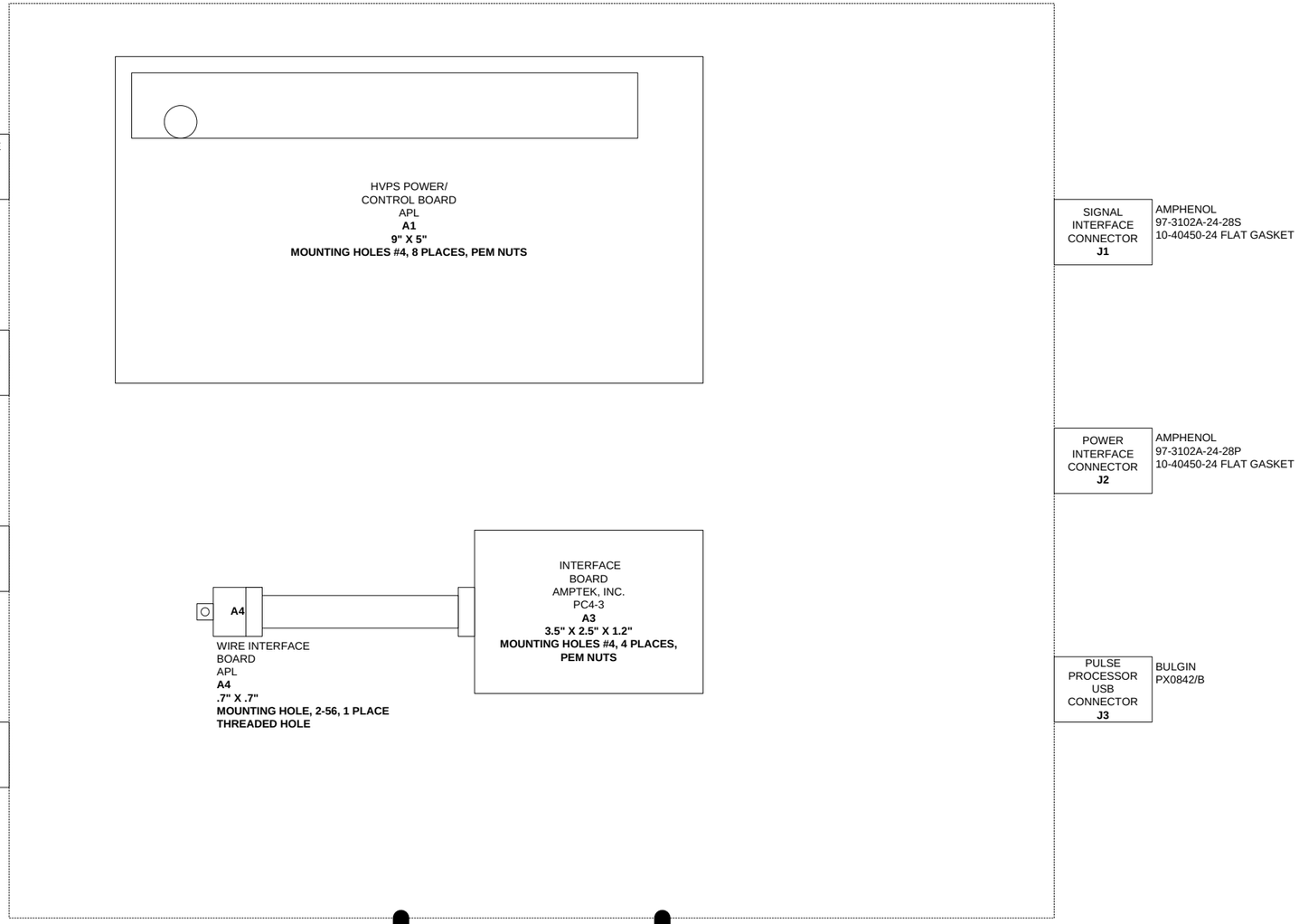
COM Port: USB
Rise: 19.2uS
Top: 0.8uS
Fast Threshold: 20
PUR Enable: PUROff
RTD ON/OFF: RTDOff
RTD Threshold: 3.13% FS
RTD Fast HWHM: 10
AutoBaseline: Off
BLR: BLR:ON DN:16 UP:4
Acquisition Mode: MCA
MCS Timebase: 10mS/channel
MCA Channels: 1024
Slow Threshold: 6.15% FS
Buffer Select: Buffer A
Gate Input (TTL): GateOff
Preset: None
Coarse Gain: 106x
Fine Gain: 1.0000
Input Polarity: Negative
Input Offset: 0.069V
Pole Zero: OFF
Det Rst Lockout: 1.64mS
TEC: 284.0K
HV: 159.7V
Preamp Power: 5.0V
Analog Out: Decimated Input
Offset: 0mV
Aux: ICR
Audio: Off


XRF HEAD
A1
W1
W1
W1
W1
P1
J4
P2
J5
P3
J6
P4
J7
XRF CONTROL
UNIT
A2
J1
P1
J2
P1
J3
P1
W2
W3
W4 (USB)
P2
J1
P2
J2
P2
J3
XRF INTERFACE
UNIT
A3
J4
P1
J5
P1
J7
P1
J6
P1
W5 (USB)
W8
W7
W6
P2
USB
GENERIC
NOTEBOOK
PC
A4
P2
AC POWER
EXTERNAL
INTERLOCK
SWITCH
A5
XRAY ACTIVE
LAMP
A6


(2) TSP, 22 AWG
6 CONTACT CONNECTOR
FILAMENT POWER/
HV RETURN/
XRF HEAD GND DETECT
CONNECTOR
P2
XRF HEAD BODY
TRANSFORMER
BAND CLAMP
POTTED ASSEMBLY
FILAMENT
TRANSFORMER
T1
SILVER
COLLIMATOR
XRAY TUBE
A4
SILVER
COLLIMATOR
GLUED TO XRF
BODY BY
CONDUCTIVE
EPOXY
A0W1
A0W1, -40KV RETURN
-40KV SHIELD
3.74K, 1/8 WATT, 1%
P7
P5
P6
2-56 THREADED HOLE LOCATED
AT BACK OF XRF HEAD,
RING TERMINAL CONNECTION
SINGLE HV CONTACT
CONNECTOR
HVPS SUPPLY
CONNECTOR
ULTRAVOLT
B200-0.187/AT22
P1
A0W1, -40KV
DETECTOR
SENSOR
FSG32MD-E2SP
AMPTEK, INC
A1
DETECTOR
BOARD
PA-230
AMPTEK, INC.
A2
J1
P2
A1W1
P1
J11
WIRING INTERFACE BOARD
APL
A3
J1
J3
J4
J7
J8
J9
J10
J5
J6
+HV
GND
TEMP
-LV
SUPPLY
(-5VDC)
+LV
SUPPLY
(+5VDC)
+TEC
-TEC
OUT
GND
MEMBRANE RIBBON CABLE
DIGIKEY
P/N FH-10U-03-ND
NOTE: MODIFICATIONS TO A2
1. REMOVE R19
6 CONDUCTOR AWG 24, SHIELDED
7 CONTACT CONNECTOR
DETECTOR
POWER
CONNECTOR
P1
A0W1
RG-178U/B
BNC CONNECTOR
DETECTOR
SIGNAL
COAX
CONNECTOR
P4
A0W1, DETECTOR SIGNAL


HIGH VOLTAGE +
CONNECTOR
ULTRAVOLT
B110US10/CA-40KV-1002
J4
(A0W1P1)
HIGH VOLTAGE WIRE SPLICE
USE PLEXIGLASS TUBING AND
EPOXY AROUND SOLDERED/
HEATSHINK SLICE
W1
HV_OUT
J1
P1
W3
SIGNAL
INTERFACE
CONNECTOR
J1
(A0W2P1)
W2
P1
J2
HVPS POWER/
CONTROL BOARD
APL
A1
J4
P1
W4, +/-15VA
+15V HVPS
P2
FILAMENT POWER/
HV RETURN/
XRF HEAD GND FAULT
DETECT
CONNECTOR
J5
(A0W1P2)
W2
P2
J3
POWER
INTERFACE
CONNECTOR
J2
(A0W3P1)
SCREW
TERMINAL
CONNECTION
TO CONTROL
UNIT
ENCLOSURE
P3
DETECTOR POWER
CONNECTOR
J6
(A0W1P3)
W5, 6 COND. + SHIELD
W4
+5VDC
NOTE: MODIFICATIONS TO A3
1. ADDED KK (22-05-3061)
CONNECTOR TO A2A3J4 USED
INSTEAD OF J4A RIBBON
CONNECTOR.
2. REPLACED R14 WITH
35.7KOHM RESISTOR.
3. REMOVED COAXIAL CABLE
FROM OUT TERMINAL.
P2
J4
J3
P2
DETECTOR SIGNAL
COAX
CONNECTOR
J7
(A0W1P4)
W6, 2 COND+SHIED 83317
P1
JP7
DIGITAL PULSE
PROCESSOR
AMPTEK, INC.
DP4
A2
JP6
P1
W7
P2
J1
INTERFACE
BOARD
AMPTEK, INC.
PC4-3
A3
J5
P1
W8, USB
P2
PULSE PROCESSOR
USB
CONNECTOR
J3
(A0W4P1)
AMPHENOL
PANEL MOUNT
ISOLATED BNC
31-10

HOFFMAN ENCLOSURE A12614SC
16" X 14" X 6"
HOFFMAN PANEL A16P14



ULTRAVOLT
B110US10/CA-40KV-1002
HIGH VOLTAGE + CONNECTOR **J4**

AMPHENOL
97-3102A-14S-6S
10-40450-16 FLAT GASKET
FILAMENT POWER/ HV RETURN/ XRF HEAD GND FAULT DETECT CONNECTOR **J5**

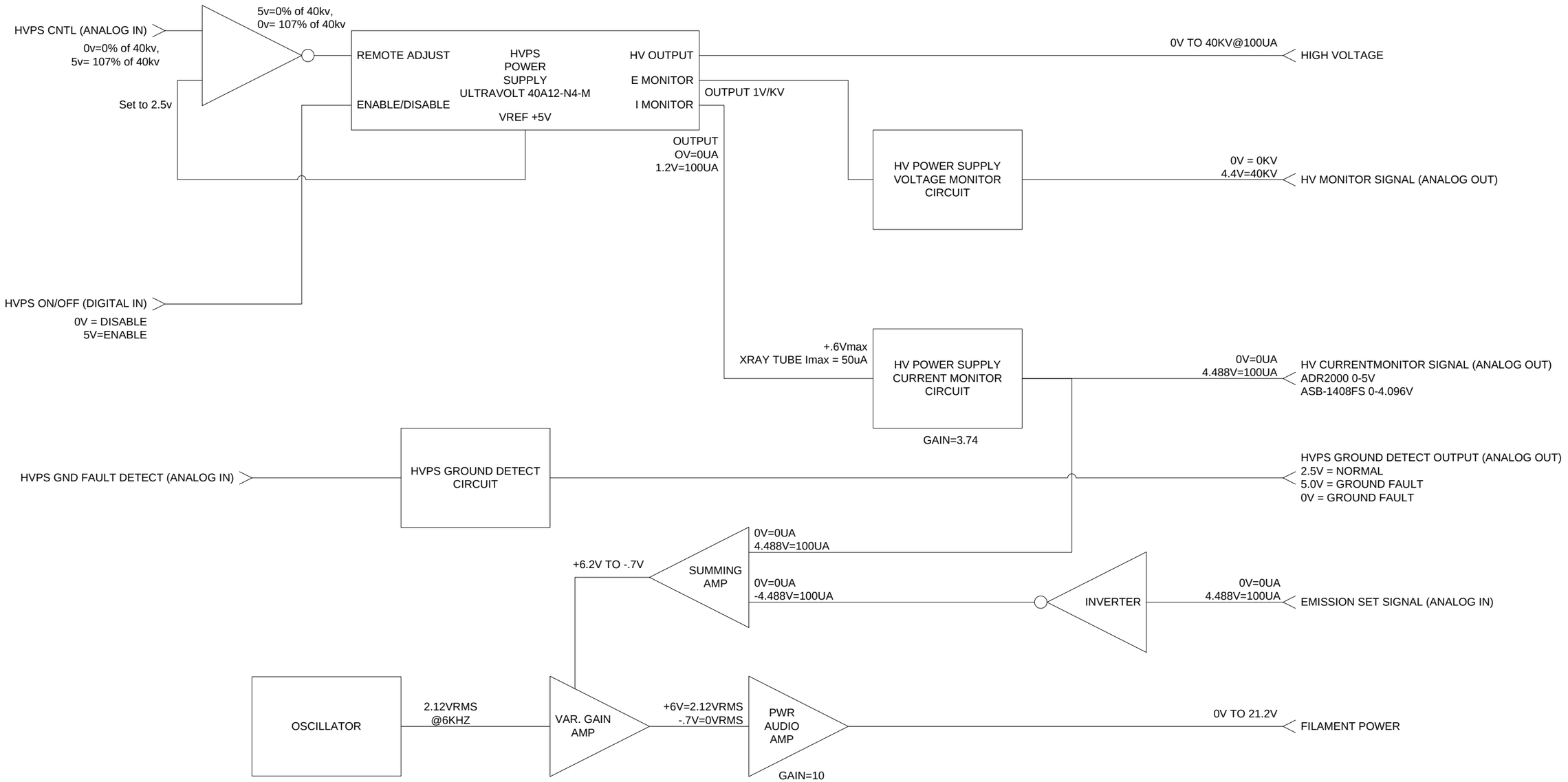
AMPHENOL
97-3102A-16S-1S
10-40450-14 FLAT GASKET
DETECTOR POWER CONNECTOR **J6**

AMPHENOL
ISOLATED BNC
31-10
DETECTOR SIGNAL COAX CONNECTOR **J7**

SIGNAL INTERFACE CONNECTOR **J1**
AMPHENOL
97-3102A-24-28S
10-40450-24 FLAT GASKET

POWER INTERFACE CONNECTOR **J2**
AMPHENOL
97-3102A-24-28P
10-40450-24 FLAT GASKET

PULSE PROCESSOR USB CONNECTOR **J3**
BULGIN
PX0842/B


HVPS CNTL (ANALOG IN)
0v=0% of 40kv,
5v= 107% of 40kv
5v=0% of 40kv,
0v= 107% of 40kv
Set to 2.5v
REMOTE ADJUST
ENABLE/DISABLE
HVPS
POWER
SUPPLY
ULTRAVOLT 40A12-N4-M
VREF +5V
HV OUTPUT
E MONITOR
I MONITOR
0V TO 40KV@100UA
HIGH VOLTAGE
OUTPUT 1V/KV
OUTPUT
OV=0UA
1.2V=100UA
HV POWER SUPPLY
VOLTAGE MONITOR
CIRCUIT
0V = 0KV
4.4V=40KV
HV MONITOR SIGNAL (ANALOG OUT)
HVPS ON/OFF (DIGITAL IN)
0V = DISABLE
5V=ENABLE
+.6Vmax
XRAY TUBE Imax = 50uA
HV POWER SUPPLY
CURRENT MONITOR
CIRCUIT
GAIN=3.74
0V=0UA
4.488V=100UA
HV CURRENTMONITOR SIGNAL (ANALOG OUT)
ADR2000 0-5V
ASB-1408FS 0-4.096V
HVPS GND FAULT DETECT (ANALOG IN)
HVPS GROUND DETECT
CIRCUIT
HVPS GROUND DETECT OUTPUT (ANALOG OUT)
2.5V = NORMAL
5.0V = GROUND FAULT
0V = GROUND FAULT
+6.2V TO -.7V
SUMMING
AMP
0V=0UA
4.488V=100UA
0V=0UA
-4.488V=100UA
INVERTER
0V=0UA
4.488V=100UA
EMISSION SET SIGNAL (ANALOG IN)
OSCILLATOR
2.12VRMS
@6KHZ
VAR. GAIN
AMP
+6V=2.12VRMS
-.7V=0VRMS
PWR
AUDIO
AMP
GAIN=10
0V TO 21.2V
FILAMENT POWER

DIGITAL SIGNALS	A6 CONNECTION
XRAY ON/OFF CMD	32 - PORT B0
SAFETY INTERLOCK MICROCONTROLLER FAIL STATUS	21 - PORT A0
XRAY ACTIVE LAMP CONNECTION STATUS	22 - PORT A1
XRAY ACTIVE LAMP STATUS	23 - PORT A2
EXCESSIVE HVPS CURRENT	24 - PORT A3
XRF HEAD GND FAULT	25 - PORT A4
EXT INTERLOCK SWITCH FAILURE STATUS	26 - PORT A5
EXT INTERLOCK SWITCH CONNECTION STATUS	27 - PORT A6
EXT INTERLOCK SWITCH STATUS	28 - PORT A7
SYSTEM GND	29 - GND

ANALOG SIGNALS	A6 CONNECTION
HVPS CONTROL	13 - D/A OUT 0
EMISSION SET	14 – D/A OUT 1

HVPS CURRENT MONITOR	1 - CH0 IN
HVPS VOLTAGE MONITOR	2 - CH1 IN
EXT. INTERLOCK SWITCH SIGNAL	4 - CH2 IN
XRF HEAD GND FAULT SIGNAL	5 - CH3 IN
+5V POWER	7 -CH4 IN
AGND	3 - AGND

SIGNALS REL TO A5		SIGNAL PASS-THRU A5
HVPS ENABLE/DISABLE	DIGITAL OUT	NO
SYSTEM GND		
HVPS CONTROL	ANALOG OUT	YES
EMISSION SET	ANALOG OUT	YES
XRF HEAD GND FAULT SIGNAL	ANALOG IN	YES
HVPS CURRENT MONITOR	ANALOG IN	YES
HVPS VOLTAGE MONITOR	ANALOG IN	YES
AGND		

+5VDC	DIGITAL PWR
+5VDC RETURN	DIGITAL PWR
+15V ANALOG	ANALOG PWR
-15 ANALOG	ANALOG PWR
+/-15 ANALOG RETURN	ANALOG PWR
+15V HVPS	ANALOG PWR
+15V HVPS RETURN	ANALOG PWR

CONTROL UNIT USB INTERFACE CONNECTOR **J3**

USB DATA ACQUISITION MODULE MEASUREMENT COMPUTING USB-1408FS **A6**

PORT Ax PORT Bx CHx IN D/A OUT x

USB HUB DLINK DUB-H4 **A1**

USB INTERFACE CONNECTOR BULGIN PX0842/B **J4**

XRAY ACTIVE WARNING LAMP CONNECTOR **J7**

EXTERNAL INTERLOCK SWITCH CONNECTOR **J6**

SAFETY INTERLOCK CONTROL BOARD APL **A5**

AC POWER CONNECTOR **J5**

AC POWER FUSE BUSSMANN HOLDER HKP-R FUSE AGC-½-R **F1**

AC POWER KEY SWITCH EAO SWITCH 704.122.0 CONTACT BLOCK 704.900.1 **S1**

AC POWER LAMP IDEC APW299D-R-120V **L1**

SCREW TERMINAL CONNECTION

TERMINAL BLOCK +5VDC **TB2**

+5VDC DIGITAL AC-DC POWER SUPPLY ACOPIAN 5EB250 **A2**

+/-15VDC ANALOG AC-DC POWER SUPPLY ACOPIAN DB15-50 **A3**

+15VDC HVPS SUPPLY AC-DC POWER SUPPLY ACOPIAN 15EB100 **A4**

TERMINAL BLOCK AC **TB1**

CONTROL UNIT SIGNAL INTEFACE CONNECTOR **J1**

CONTROL UNIT POWER CONNECTOR **J2**

W1 W2 W3 W4 W5 W6 W7 W8 W9 W10 W11 W12 W13 W14 W15 W16 W17

HOFFMAN ENCLOSURE A12614SC
16" X 14" X 6"
HOFFMAN PANEL A16P14

AMPHENOL
97-3102A-24-28S
10-40450-24 FLAT GASKET

CONTROL UNIT
SIGNAL
INTEFACE
CONNECTOR
J1

AMPHENOL
97-3102A-24-28P
10-40450-24 FLAT GASKET

CONTROL UNIT
POWER
CONNECTOR
J2

BULGIN
PX0842/A

CONTROL UNIT
USB
INTERFACE
CONNECTOR
J3

J1-AC

J2
LAMP

SAFETY
INTERLOCK CONTROL
BOARD
APL
A5
4" X 4.5"
MOUNTING HOLES #4, 4 PLACES, PEM NUTS

J3

J4
ANALOG DAQ

J5
DIGITAL DAQ

ANALOG IN/OUT

USB DATA
ACQUISITION MODULE
MEASUREMENT
COMPUTING
USB-1408FS
3.11" X 3.22" X 1"
A6
PEM NUTS

USB
CONNECTOR

PORTS A&B

USB
CONNECTOR

USB
CONNECTOR

USB HUB
DLINK
DUB-H4
4.06" X 2.5" X 1.125"
A1
GLUE A1 TO G10
SUBSTRATE WHICH IS
SCREWED TO PLATE
PEM NUTS

USB
CONNECTOR

+5VDC
DIGITAL AC-DC
POWER SUPPLY
ACOPIAN
5EB250
3.5" X 2.5" X 2.375
A2
MOUNT WITH THRU HOLE

+/-15VDC
ANALOG
AC-DC
POWER
SUPPLY
ACOPIAN
DB15-50
3.5" X 2.5" X 2.375
A3
MOUNT WITH THRU HOLE

+15VDC
HVPS SUPPLY
AC-DC
POWER SUPPLY
ACOPIAN
15EB100
3.5" X 2.5" X 2.375
A4
MOUNT WITH THRU HOLE

TERMINAL
BLOCK
+5VDC
TB2
PEM NUTS

TERMINAL
BLOCK
AC
TB1
PEM NUTS

EXTERNAL
INTERLOCK
SWITCH
CONNECTOR
J6

AMPHENOL
97-3102A-14S-2P
10-40450-14 FLAT GASKET

XRAY ACTIVE
WARNING
LAMP
CONNECTOR
J7

AMPHENOL
97-3102A-14S-2S
10-40450-14 FLAT GASKET

AC POWER
CONNECTOR
J5

AMPHENOL
97-3102A-16-10P
10-40450-10 FLAT GASKET

USB
INTERFACE
CONNECTOR
J4

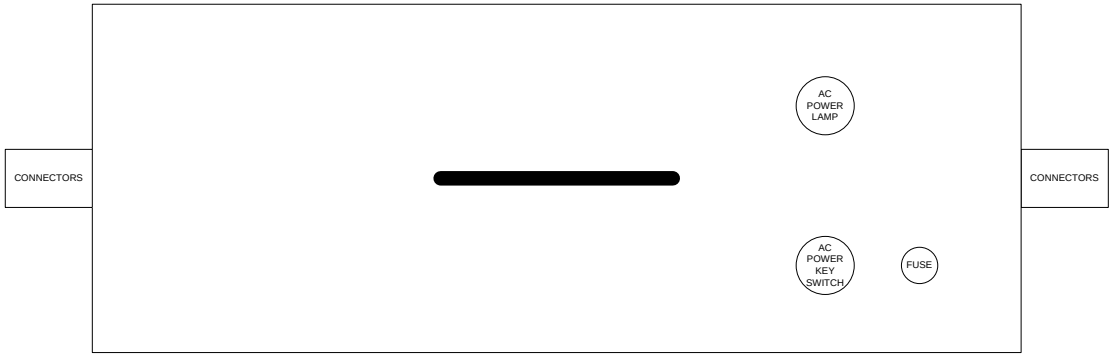
BULGIN
PX0842/B

KEYSTONE
OVAL HANDLE
PN 7186

KEY LOCK POWER
SWITCH
EAO 704.122.0

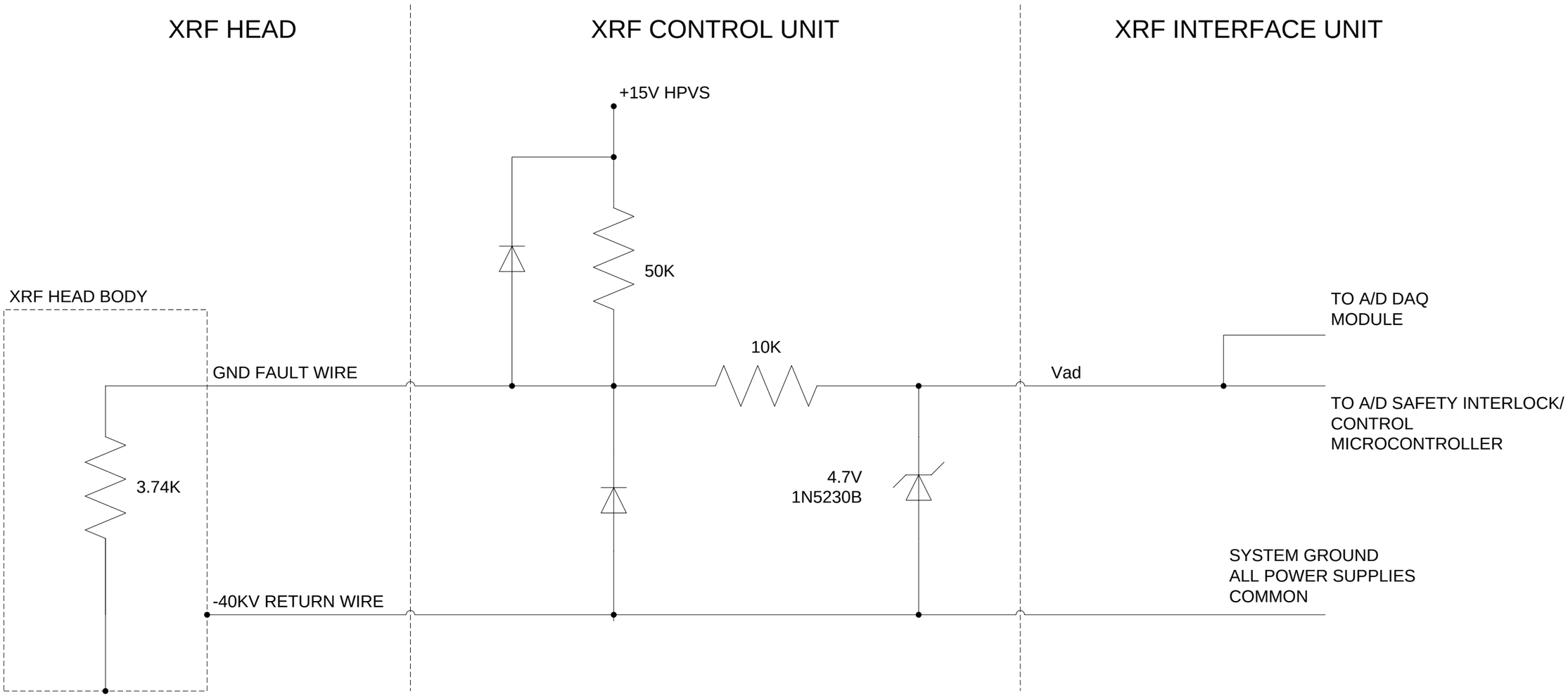
PILOT LIGHT
IDEC APW299D-R-120V

FUSE HOLDER
BUSSMANN HKP-R


AC
POWER
LAMP
CONNECTORS
CONNECTORS
AC
POWER
KEY
SWITCH
FUSE

FRONT VIEW

BOREHOLE XRF – SIMPLIFIED SCHEMATIC OF XRF HEAD GROUND FAULT DETECT CIRCUIT



CONDITIONS:
1) NORMAL, Vad ~= 1Vdc

2) -40KV RETURN WIRE OPEN IN CABLE OR XRF HEAD, Vad ~=4.7Vdc

3) GND FAULT WIRE OPEN IN CABLE OR XRF HEAD, Vad ~=4.7Vdc

XRF INTERFACE UNIT A0A3

USB TYPE A

BULGIN PX0842/B

USB TYPE B

USB TYPE A

HOST PC

USB TYPE B

MEASUREMENT COMPUTING USB-1408FS

USB TYPE A

USB TYPE B

D-LINK 4 PORT HUB

USB TYPE A

USB TYPE B

BULGIN PX0842/A

USB TYPE A

XRF CONTROL UNIT A0A2

USB TYPE B

BULGIN PX0842/B

USB TYPE A

USB TYPE B

PULSE PROCESSOR

REVISIONS				
ZONE	REV	DESCRIPTION	DATE:	APPROVED

CONTROLLER PROGRANNING PINS

VPP +5V GND ICSPDAT/PGD ICSPCLK/PGC AUX

STATUS LEDS

R9-A 270 D2 EXT INTERLOCK SWITCH STATUS
R9-B 270 D3 EXT INTERLOCK SWITCH CONNECT STATUS
R9-C 270 D4 EXT INTERLOCK SWITCH FAILURE STATUS
R9-D 270 D5 XRF HEAD GND FAULT
R9-E 270 D6 EXCESSIVE HVPS CURRENT
R9-F 270 D7 XRAY ACTIVE LAMP STATUS
R9-G 270 D8 XRAY ACTIVE LAMP CONNECT STATUS
R9-H 270 D9 SAFTEY INTERLOCK MICROCONTROLLER FAIL STATUS

ANALOG IN/OUT

J4-1 HVPS CONTROL
J4-2 EMISSION SET
J4-3 HVPS CURRENT MONITOR
J4-4 HVPS VOLTAGE MONITOR
J4-5 EXT.INTERLOCK SWITCH SIGNAL
J4-6 XRF HEAD GND FAULT SIGNAL
J4-7 GND
J4-8 GND
J4-9 GND
J4-10 GND
J4-11 GND
J4-12 GND

PORT A PORT C LOW PORT C UPPER

SAFETY INTERLOCK MICROCONTROLLER

U2 PIC16F886

XRAY ACTIVE LAMP RELAY

K1 MCK240D5
XRAY ACTIVE LAMP OFF/ON
F1 1A FS1 FS2

ANALOG IN /OUT,
XRAY ON/OFF,
HEAD GROUND DETECT

J3-1 HVPS CONTROL
J3-2 EMISSION SET
J3-3 HVPS CURRENT MONITOR
J3-4 HVPS VOLTAGE MONITOR
J3-5 XRF HEAD GND FAULT SIGNAL
J3-6 HVPS OFF/ON
J3-7 GND
J3-8 GND
J3-9 GND
J3-10 GND
J3-11 GND
J3-12 GND

U3 LMV771 ACI_OUT
U1 LTC1966
T1 CSE187L 61A 2A
R1 1k R2 100k R3 100k C9 .1UFD C8 .01UFD C1 1.0UFD

CURRENT MONITOR XFER

CURRENT MONITOR RMS TO DC CONVERTER

XRAY ACTIVE LAMP CURRENT OUTPUT
GOOD CURRENT = ??V
NO CURRENT = 0V

XRAY ACTIVE LAMP AC

XRAY ACTIVE LAMP HOT J1-1
XRAY ACTIVE LAMP RET J1-3

XRAY ACTIVE LAMP CONNECT STATUS
NO CONNECTION J1-4 = 0v
CONNECTION J1-4 = 5V

XRAY ACTIVE LAMP CONNECT SENSOR

R8 10k XRAY ACTIVE LAMP CONNECT J8-1
XRAY ACTIVE LAMP CONNECT J8-2
R12 100K

DIGITAL STATUS IN/OUT

J5-1 XRAY ON/OFF
J5-2 SAFETY INTERLOCK MICROCONTROLLER FAIL STATUS
J5-3 XRAY ACTIVE LAMP CONNECT STATUS
J5-4 XRAY ACTIVE LAMP STATUS
J5-5 EXCESSIVE HVPS CURRENT
J5-6 XRF HEAD GND FAULT
J5-7 EXT INTERLOCK SWITCH FAILURE STATUS
J5-8 EXT INTERLOCK SWITCH CONNECT STATUS
J5-9 EXT INTERLOCK SWITCH STATUS
J5-10
J5-11
J5-12

EXTERNAL INTERLOCK SWITCH

R5 10k SWITCH J2-1
SWITCH RET J2-2
R6 10k CONNECT J2-3
CONNECT RET J2-4
R7 20K

EXT INTERLOCK SWITCH
NOTE: 20K RESISTOR IN SERIES
AND CO-LOCATED WITH SWITCH.

EXT INTERLOCK SWITCH OUTPUT
SWITCH OPEN J2-2 = 0v
SWITCH CLOSED J2-2 = 2.0v
SWTICH CABLE SHORTED J2-2 = 3.3v

EXT INTERLOCK SWITCH CONNECT STATUS
NO CONNECTION J2-4 = 0v
CONNECTION J2-4 = 5v

R11 100K

POWER +5V

J6-1 +5V
J6-2 GND
C2 47ufd C11 .1UFD C4 .1UFD C5 .1UFD C6 .1UFD C7 .01UFD

ADDED TO PROTOTYPE AREA

PC6 PIC TX
PC7 PIC RX
U4 MAX233
RS232 TX J9-1
RS232 RX J9-2
GND J9-3

APPLIED PHYSICS LABORATORY	
CONTRACT NO.	
DIRECTOR	
PROJ ENGR	ELAM
ENGINEER	LIGHT
CHECKED:	
DRAWN:	SABIN
APPLICATION DATA	
NEXT ASSY.	USED ON

APPLIED PHYSICS LABORATORY
UNIVERSITY OF WASHINGTON
SEATTLE WASHINGTON

TITLE: SAFETY INTERLOCK/CONTROL BRD, A0A3A5, SCHEMATIC, XRF INTERFACE UNITA0A3, BOREHOLE XRF PROTOTYPE

SIZE: | CODE: 98514 | DRAWING NO:

DATE: 26 APR 2007

REVISIONS				
ZONE	REV	DESCRIPTION	DATE:	APPROVED
B3	A.2	FIXED ERROR R27 AND U10	5/4/07	PLS
A4	A.3	ADDED RESISTOR AND DIODE	6/11/07	PLS

NOTE:
1. ADDED PROTECTION CIRCUIT FOR HVPS.
2. CUT BETWEEN U3-6 AND TP14.
3. ADDED RESISTOR AND DIODE AT CUT.

TP14 HVPS CONTROL VOLTAGE
5V = 0KV; 0V=42.8KV

TP30 HVPS CONTROL VOLTAGE
0V = 0KV; 4.096V = 42.8KV

HVPS

HVPS VOLTAGE MONITOR
10KV=10V; 40KV=40V +/-2.5%

VOLTAGE MONITOR CIRCUIT

NOTE:
JP1 CONNECTED TO REDUCE NOISE ON X-RAY DETECTOR.

HVPS VOLTAGE MONITOR
10KV=1.1V; 40KV=4.4V +/-2.5%

XRF HEAD GND FAULT SIGNAL
HV RTN
HV RTN
HV RTN

HVPS CONTROL
EMISSION SET
HVPS CURRENT MONITOR
HVPS VOLTAGE MONITOR
XRF HEAD GND FAULT SIGNAL
HVPS OFF/ON
GND
GND
GND
GND
GND
GND

CURRENT MONITOR CIRCUIT

HVPS CURRENT MONITOR
0 TO 100UA = 0 TO 1.2 VOLTS

HVPS CURRENT MONITOR
0 TO 100UA = 0 TO 4.49 VOLTS

POWER OUTPUT

CURRENT EMISSION SUMMER

MODIFIED SEE NOTE

NOTE:
1. MODIFIED DRAWING DUE TO AN ERROR.
2. CUT TRACE BETWEEN R27 AND U10-14.
3. ADDED TRACE BETWEEN R27AND U10-12

+15VHVPS
+15VA
-15VA
GND
GND
GND

OSCILLATOR

VARIABLE GAIN AMP

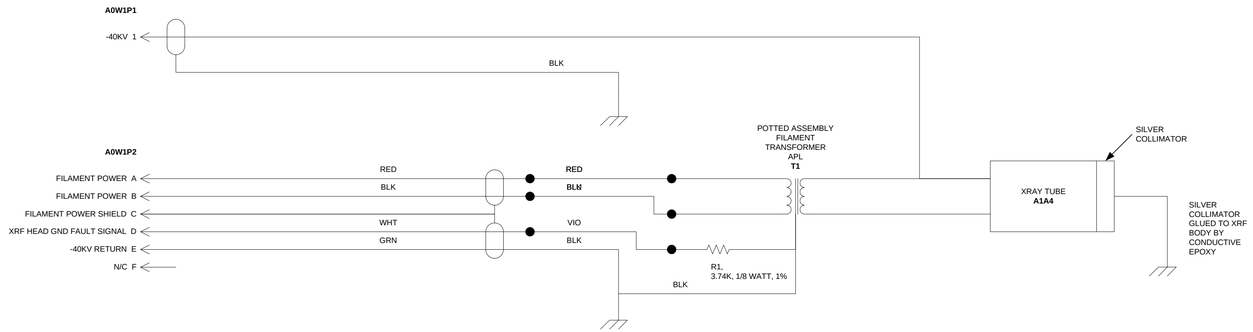
W=((X1-X2)(Y1-Y2)/10V)+Z

APPLIED PHYSICS LABORATORY	
CONTRACT NO.	
DIRECTOR	
PROJ ENGR	ELAM
ENGINEER	LIGHT
CHECKED:	
DRAWN:	SABIN
APPLICATION DATA	
NEXT ASSY.	USED ON

APPLIED PHYSICS LABORATORY
UNIVERSITY OF WASHINGTON
SEATTLE WASHINGTON

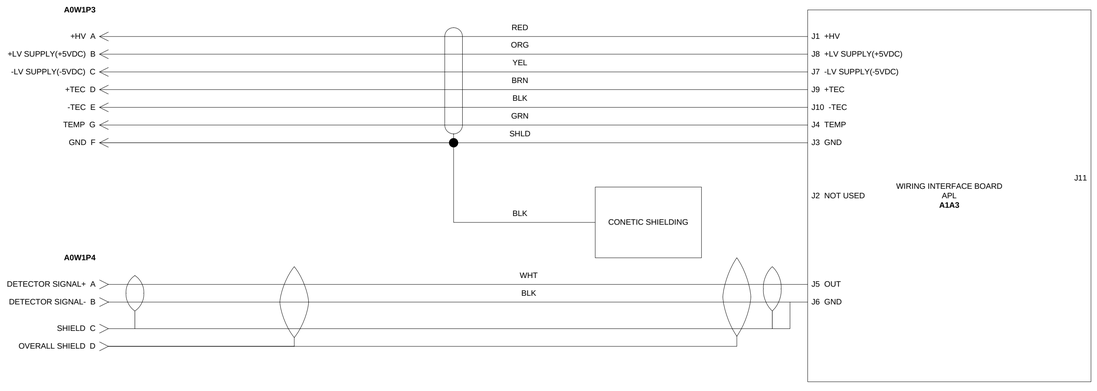
TITLE:
HVPS POWER/CONTROL BRD A0A2A1, SCHEMATIC,
XRF CONTROL UNITA0A2,
BOREHOLE XRF PROTOTYPE

SIZE:	CODE:	DRAWING NO:
	98514	
DATE:	27 JULY 2007	



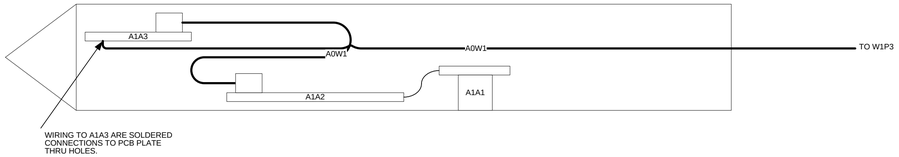
NOTE:
CONTACT ORDERING NOT SEQUENTIAL

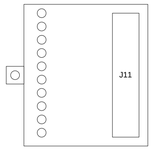
NOTE:
CONTACT ORDERING NOT SEQUENTIAL ON J1-J10



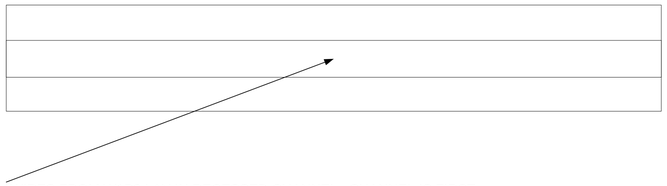
CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON			
	XRF HEAD UMBILICAL, SCHEMATIC A0W1, SYSTEM LEVEL, BOREHOLE XRF PROTOTYPE			
DRAWN BY: LIGHT	SIZE: D	CAGE CODE: 98514	DWG NO: XXXXX	REV:
FILENAME: BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	DATE: 22AUG07		SHEET: 1 OF 1	

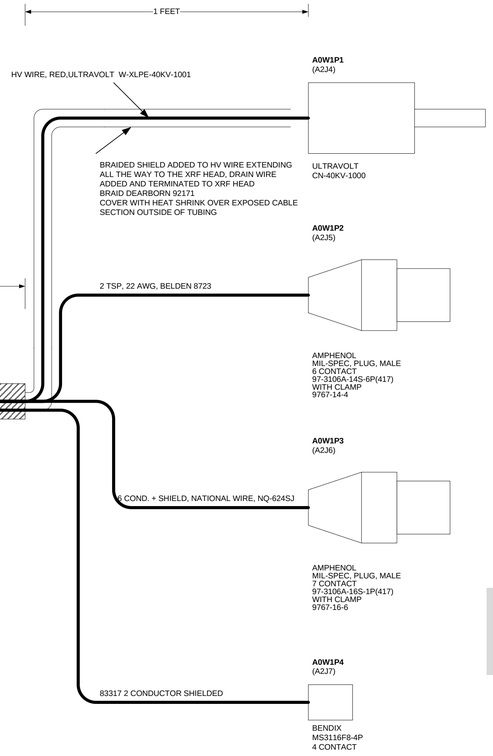
A1A3 WIRING DETAIL





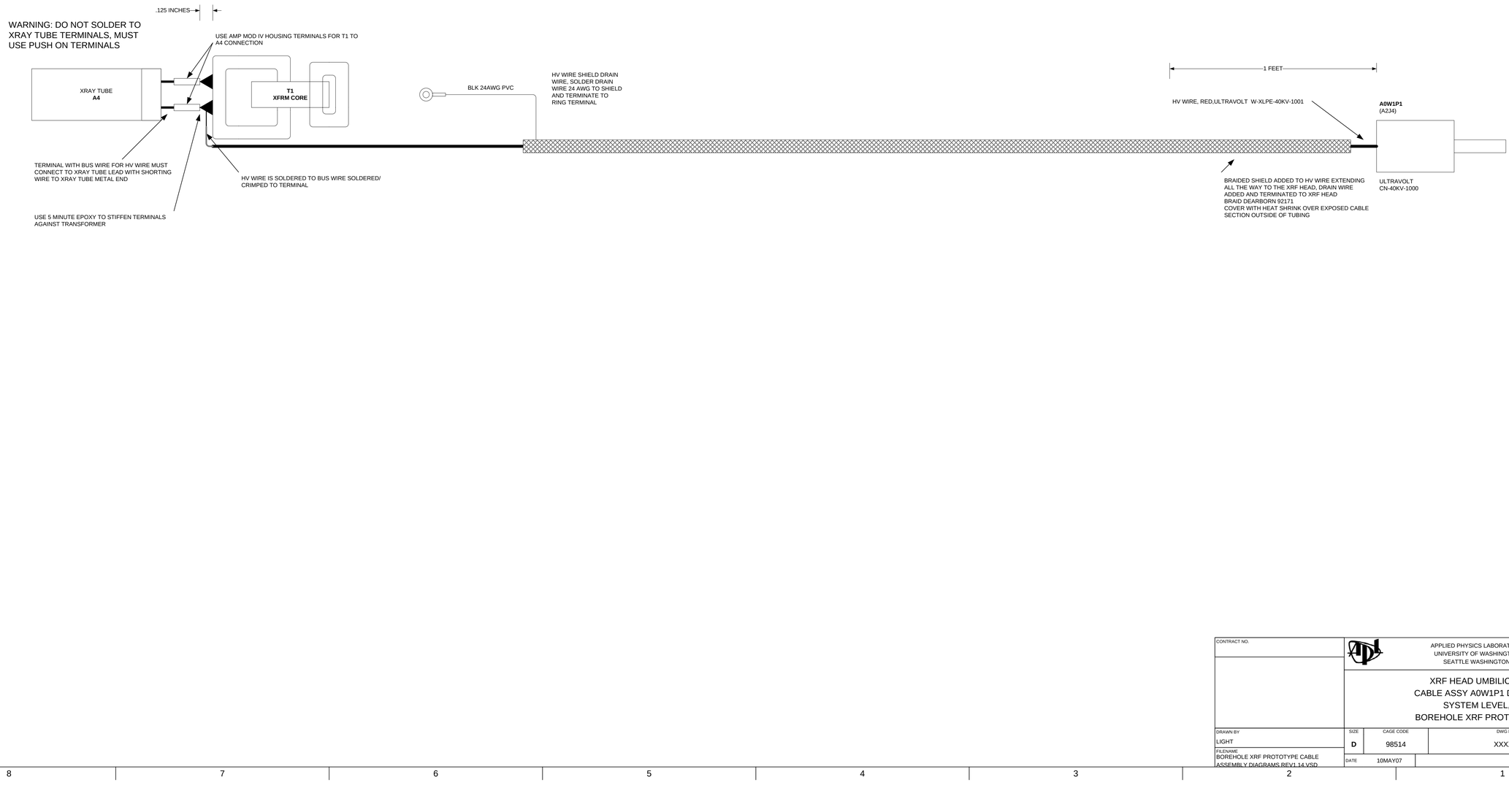
WIRING INTERFACE BOARD
APL
A1A3





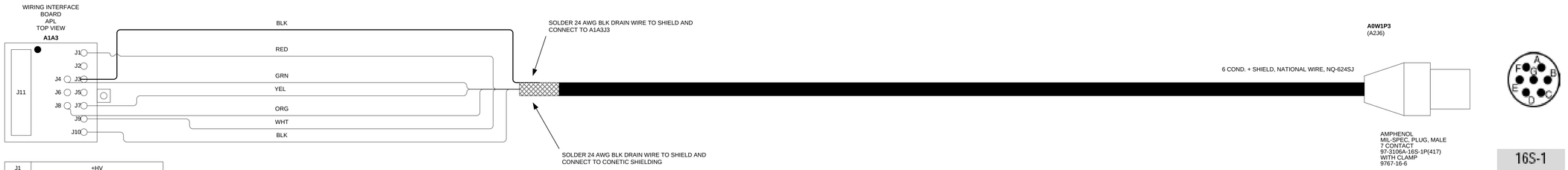
NOTES
1) REFER TO “Borehole XRF Head Process Assembly RevX.X” FOR DETAILED XRF HEAD ASSEMBLY AND WIRING INFORMATION.

CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON			
	XRF HEAD UMBILICAL, CABLE ASSY A0W1, SYSTEM LEVEL, BOREHOLE XRF PROTOTYPE			
DRAWN BY LIGHT	SIZE D	CAGE CODE 98514	DWG NO XXXXX	REV
FILENAME BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	DATE 22AUG07		SHEET 1 OF 3	

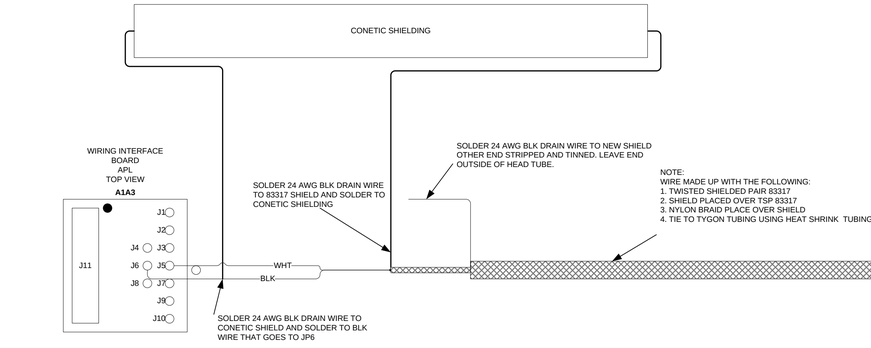


CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON			
	XRF HEAD UMBILICAL, CABLE ASSY A0W1P1 DETAIL, SYSTEM LEVEL, BOREHOLE XRF PROTOTYPE			
DRAWN BY: LIGHT	SIZE: D	CAGE CODE: 98514	DWG NO: XXXXX	REV:
FILENAME: BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	DATE: 10MAY07		SHEET: 2 OF 5	

CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON		
	XRF HEAD UMBILICAL, CABLE ASSY A0W1P2 DETAIL, SYSTEM LEVEL, BOREHOLE XRF PROTOTYPE		
DRAWN BY: LIGHT	SIZE: D	CAGE CODE: 98514	DWG NO: XXXXX	REV:
FILENAME: BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	DATE: 15MAY07		SHEET: 3 OF 3



J1	+HV
J2	NOT USED
J3	GND
J4	TEMP
J5	OUT
J6	GND
J7	-LV SUPPLY(-5VDC)
J8	+LV SUPPLY (+5VDC)
J9	+TEC
J10	-TEC



NOTES:
1) REMOVE OUTER JACKET AND SHIELD FROM NATIONAL WIRE, NQ-624SJ BEFORE ROUTING DOWN XRF HEAD CABLE CHANNEL.
2) SOLDER DRAIN WIRE, 24 AWG BLK, TO SHIELD THEN SOLDER TO BLK WIRE OF THE TWISTED WIRE THEN TO PCB.
3) INSTALL 3MIL KAPTON INSULATION INTO WIRING CHANNEL USING CUSTOM TOOL
4) INSTALL CONETIC SHIELDING FOIL OVER KAPTON WITH CUSTOM TOOL
5) LAY CABLES INTO CHANNEL AND FOLD OVER KAPTON AND CONETIC FOIL, HOLD IN PLACE WITH RUBBER BANDS UNTIL FINAL ASSEMBLY WITH HEAD HOUSING

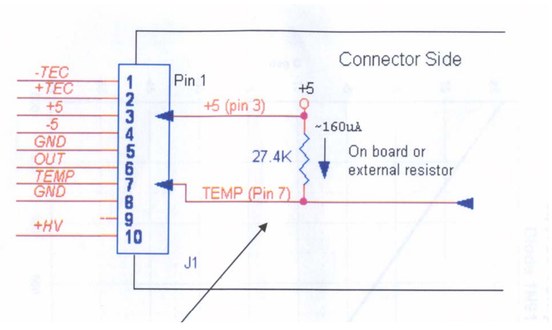
CONTRACT NO.

APPLIED PHYSICS LABORATORY
UNIVERSITY OF WASHINGTON
SEATTLE WASHINGTON

XRF HEAD UMBILICAL, CABLE ASSY A0W1P3 AND A0W1P4 DETAIL, SYSTEM LEVEL, BOREHOLE XRF PROTOTYPE

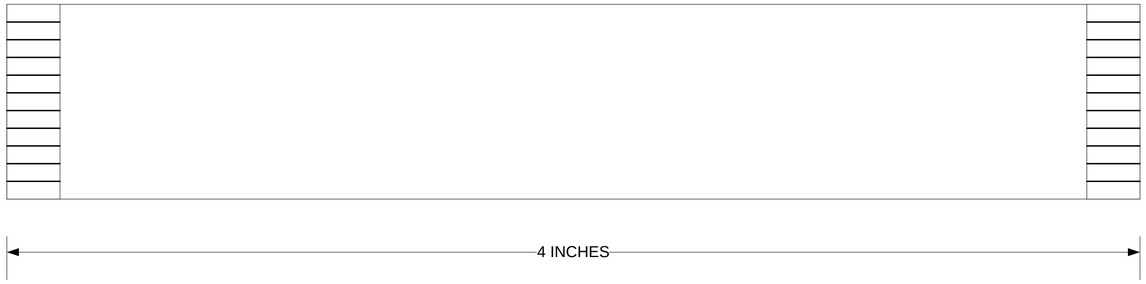
DRAWN BY: LIGHT
FILENAME: BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD
SIZE: D
CAGE CODE: 98514
DWG NO: XXXXX
REV:
DATE: 22AUG07
SHEET: 2 OF 3

A1W1P1		A1W1P2
-TEC 10	⟵	1 -TEC
+TEC 9	⟵	2 +TEC
+LV SUPPLY (+5VDC) 8	⟵	3 +LV SUPPLY (+5VDC)
-LV SUPPLY(-5VDC) 7	⟵	4 -LV SUPPLY (-5VDC)
GND 6	⟵	5 GND
OUT 5	⟵	6 OUT
TEMP 4	⟵	7 TEMP
GND 3	⟵	8 GND
NOT USED 2	⟵	9 NOT USED
+HV 1	⟵	10 +HV



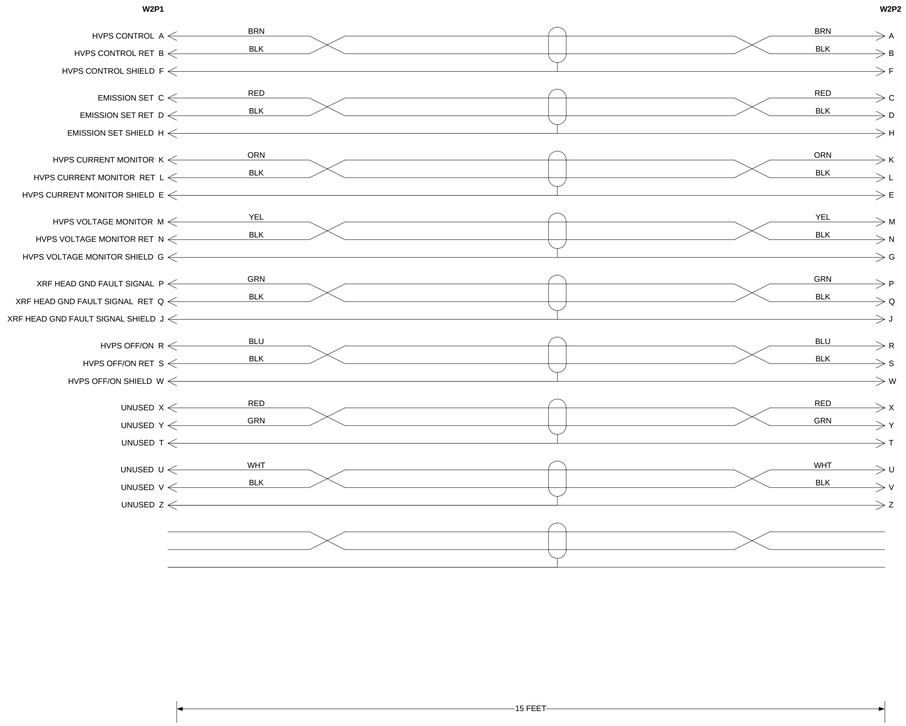
A1W1P1 (A1A3J11) — **A1W1P2 (A1A2J1)**

FLEXIBLE, FLAT RIBBON CABLE, PROVIDED BY AMPTEK, INC

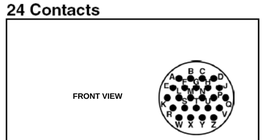


NOTE
THE MATING CONNECTORS FOR THIS CABLE ASSEMBLY FACE IN OPPOSITE DIRECTIONS WHICH RESULTS IN A INVERSE MAPPING OF THE CONNECTOR NUMBERING. E.G. PIN1, A1A3J11 MAPS TO PIN 10 OF A1A2J1. THE ABOVE SCHEMATIC REFLECTS THIS MAPPING.

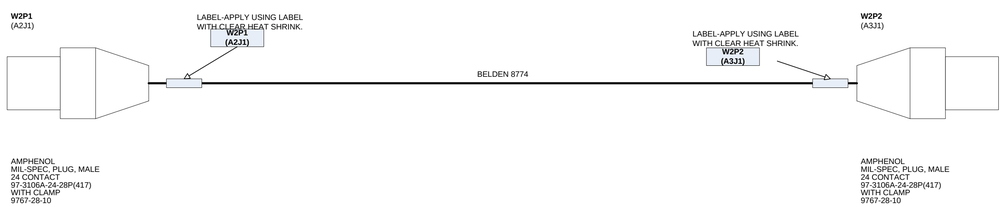
CONTRACT NO.		APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON	
		DETECTOR INTERFACE, CABLE ASSY A1W1, XRF HEAD, BOREHOLE XRF PROTOTYPE	
DRAWN BY LIGHT			
FILENAME BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	SIZE B	CAGE CODE 98514	DWG NO XXXXX / REV
	DATE 23APR07		SHEET 1 OF 1



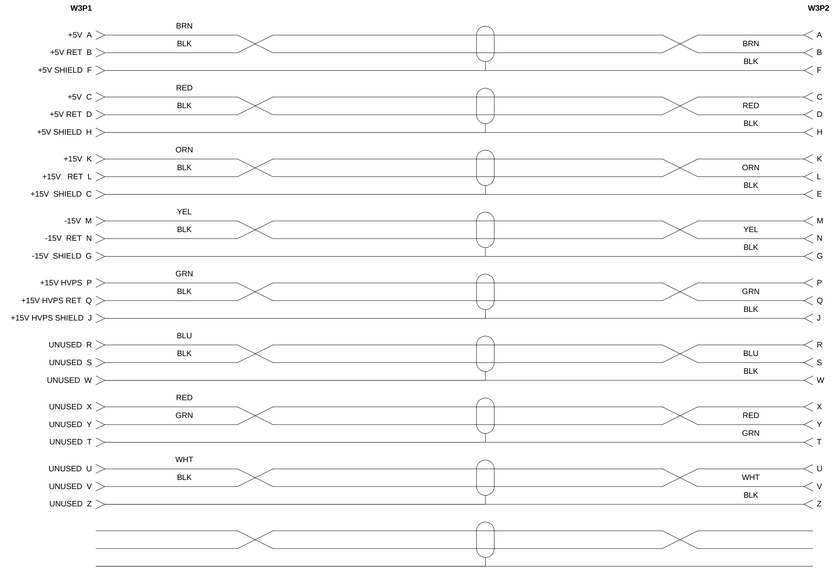
24 Contacts



Insert Arrangement	24-28
Contacts	24#16
Service Rating	INST.



CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON				
	DECKBOX INTERCONNECT-SIGNAL, CABLE ASSY A0W2, SYSTEM LEVEL, BOREHOLE XRF PROTOTYPE				
DRAWN BY LIGHT	SIZE D	CAGE CODE 98514	DWG NO XXXXX	REV	
FILENAME BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	DATE 21MAY07		SHEET 7 OF 1		



24 Contacts

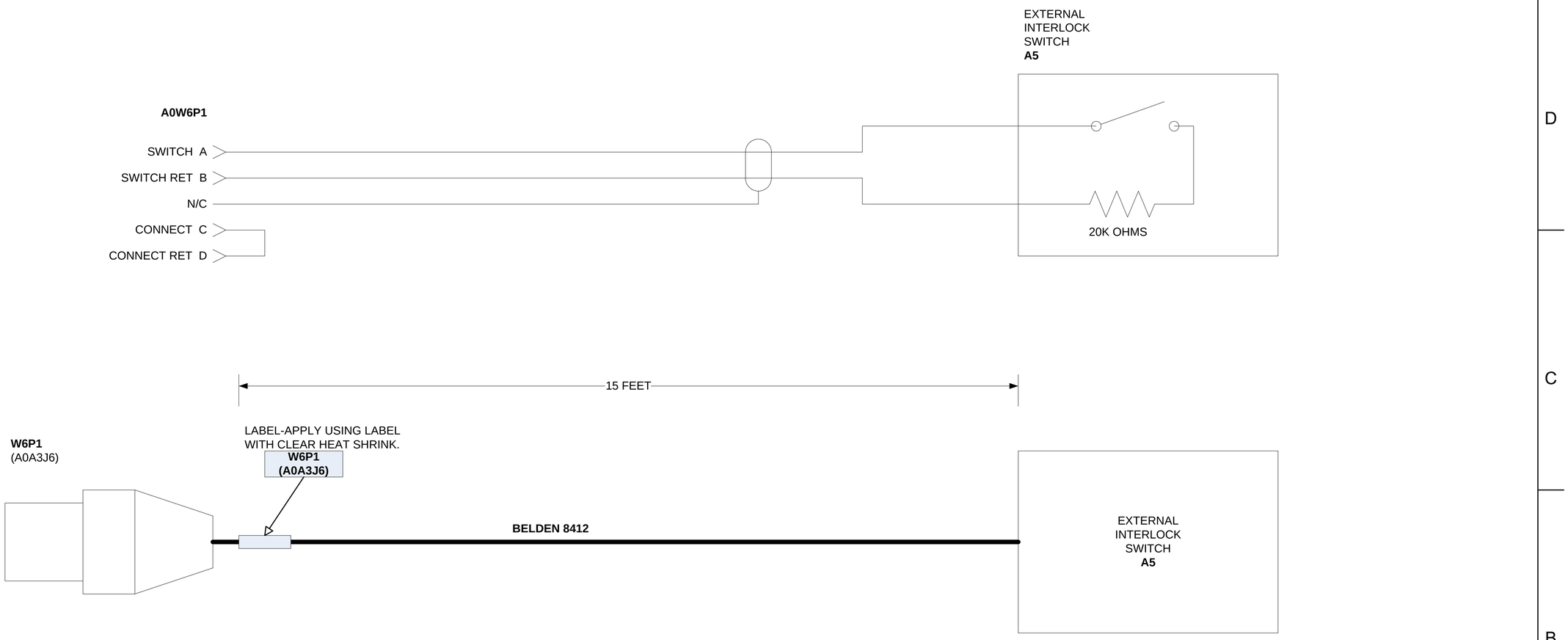
FRONT VIEW

Insert Arrangement	24-28
Contacts	24#16
Service Rating	INST.

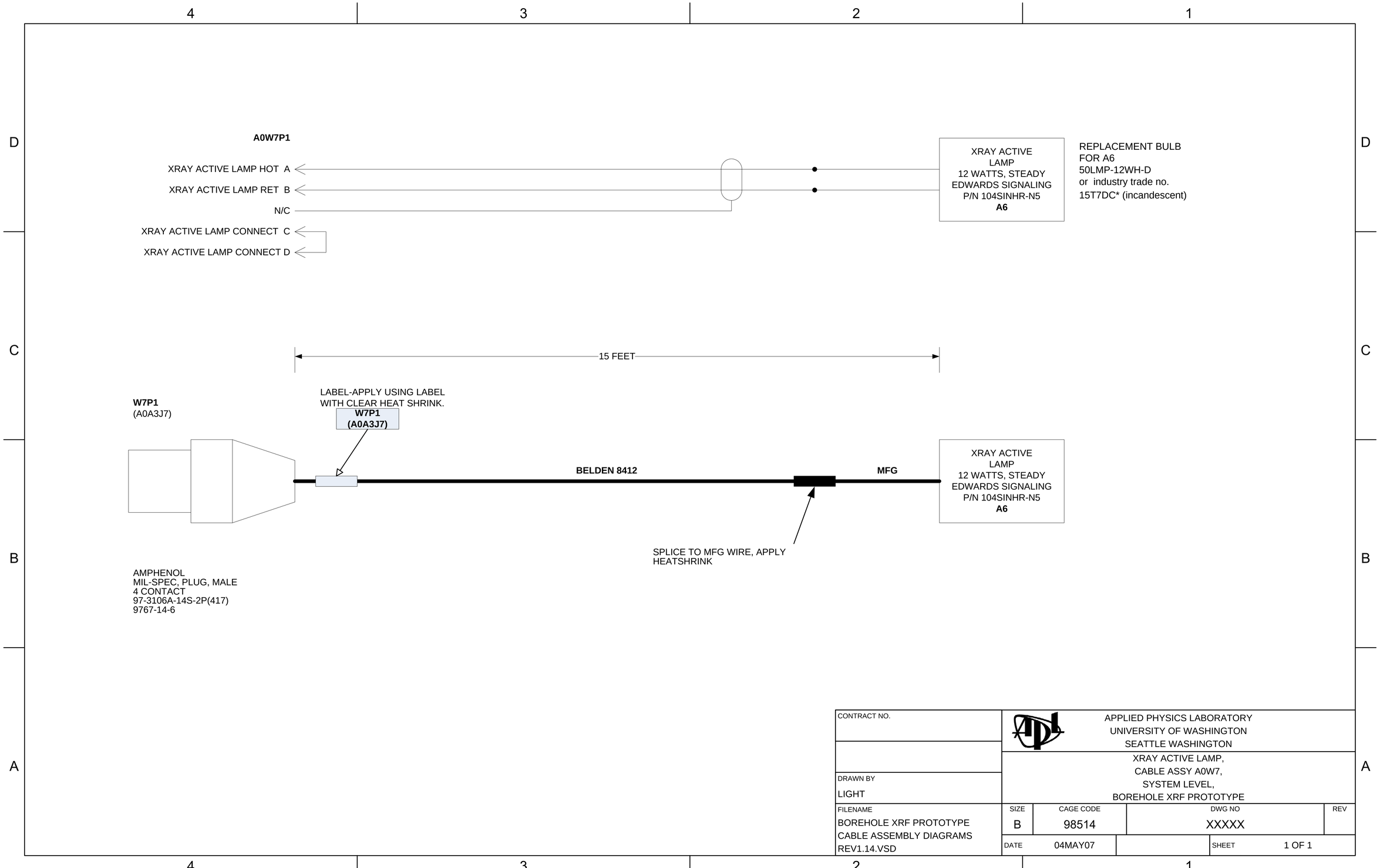
AMPHENOL
MIL-SPEC, PLUG, FEMALE
24 CONTACT
97-3106A-24-28S(417)
WITH CLAMP
9767-28-10

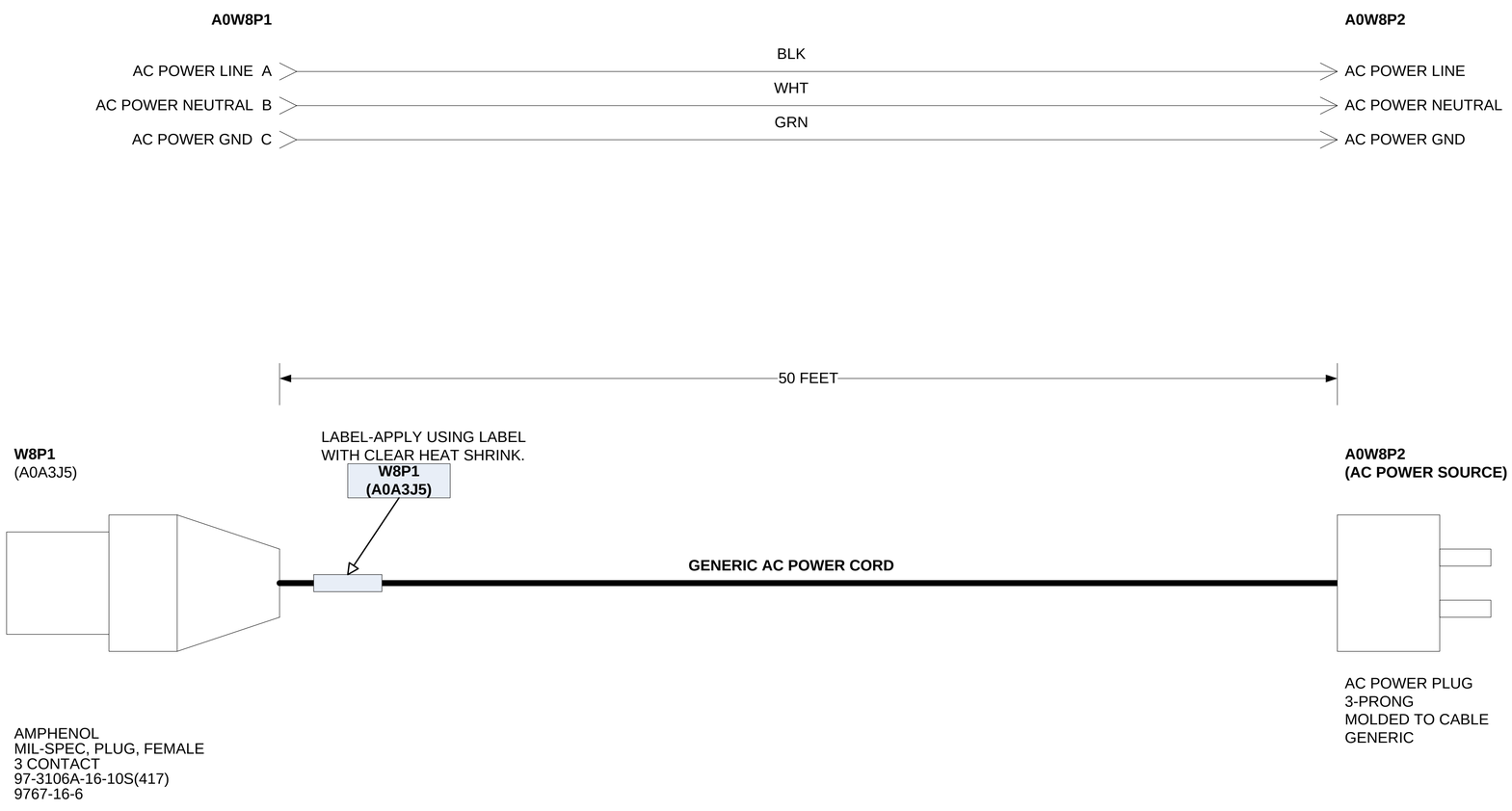
AMPHENOL
MIL-SPEC, PLUG, FEMALE
24 CONTACT
97-3106A-24-28S(417)
WITH CLAMP
9767-28-10

CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON			
	DECKBOX INTERCONNECT-POWER, CABLE ASSY A0W3, SYSTEM LEVEL, BOREHOLE XRF PROTOTYPE			
DRAWN BY LIGHT	SIZE D	CAGE CODE 98514	DWG NO XXXXX	REV
FILENAME BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	DATE 21MAY07		SHEET 8 OF 1	

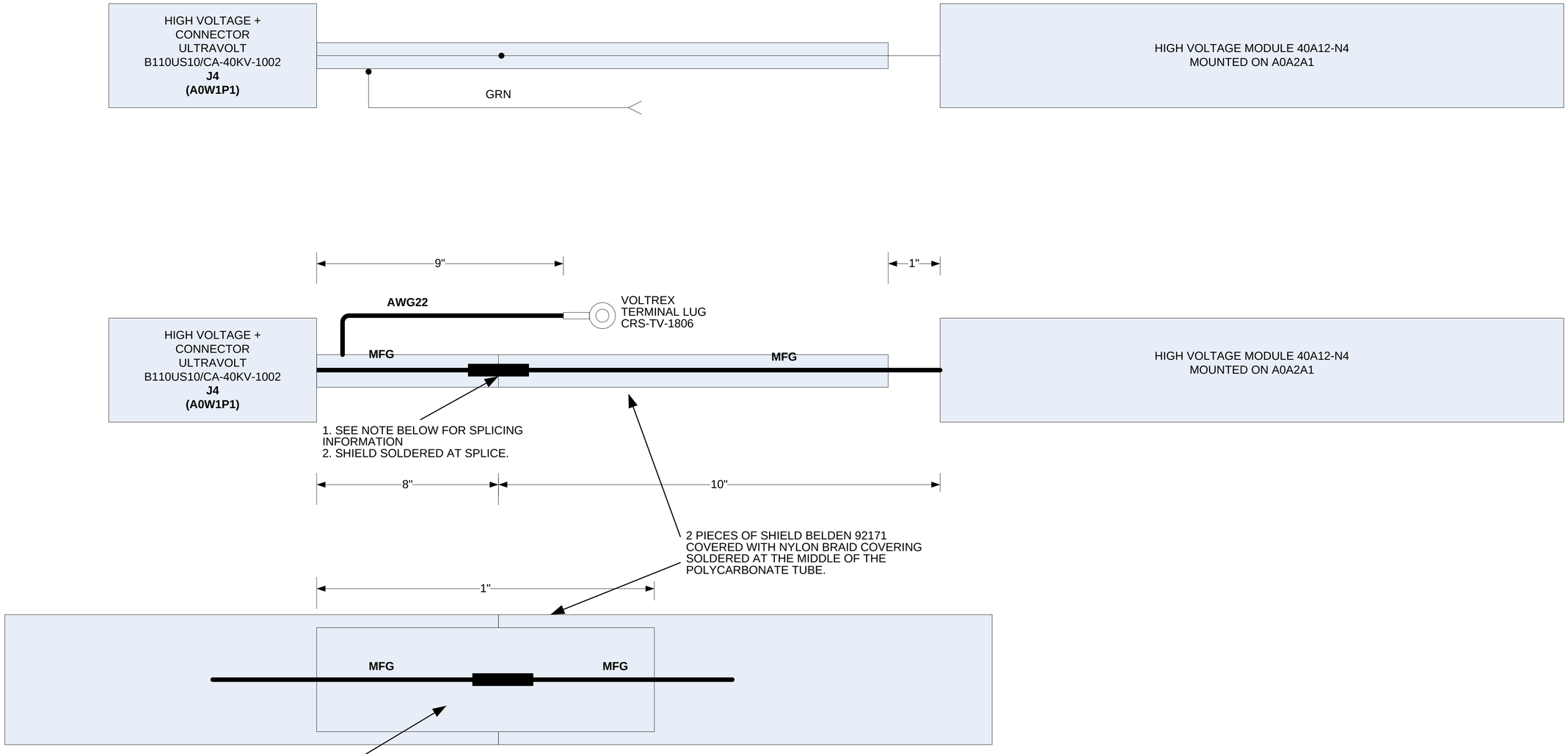


CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON			
DRAWN BY LIGHT	EXTERNAL INTERLOCK SWITCH, CABLE ASSY A0W6, SYSTEM LEVEL, BOREHOLE XRF PROTOTYPE			
FILENAME BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	SIZE B	CAGE CODE 98514	DWG NO XXXXX	REV
	DATE 04MAY07		SHEET 1 OF 1	


A0W7P1
XRAY ACTIVE LAMP HOT A
XRAY ACTIVE LAMP RET B
N/C
XRAY ACTIVE LAMP CONNECT C
XRAY ACTIVE LAMP CONNECT D
XRAY ACTIVE LAMP
12 WATTS, STEADY
EDWARDS SIGNALING
P/N 104SINHR-N5
A6
REPLACEMENT BULB
FOR A6
50LMP-12WH-D
or industry trade no.
15T7DC* (incandescent)
15 FEET
W7P1
(A0A3J7)
LABEL-APPLY USING LABEL
WITH CLEAR HEAT SHRINK.
W7P1
(A0A3J7)
BELDEN 8412
MFG
XRAY ACTIVE
LAMP
12 WATTS, STEADY
EDWARDS SIGNALING
P/N 104SINHR-N5
A6
SPLICE TO MFG WIRE, APPLY
HEATSHRINK
AMPHENOL
MIL-SPEC, PLUG, MALE
4 CONTACT
97-3106A-14S-2P(417)
9767-14-6
CONTRACT NO.
DRAWN BY
LIGHT
FILENAME
BOREHOLE XRF PROTOTYPE
CABLE ASSEMBLY DIAGRAMS
REV1.14.VSD
APPLIED PHYSICS LABORATORY
UNIVERSITY OF WASHINGTON
SEATTLE WASHINGTON
XRAY ACTIVE LAMP,
CABLE ASSY A0W7,
SYSTEM LEVEL,
BOREHOLE XRF PROTOTYPE
SIZE
B
CAGE CODE
98514
DWG NO
XXXXX
REV
DATE
04MAY07
SHEET
1 OF 1

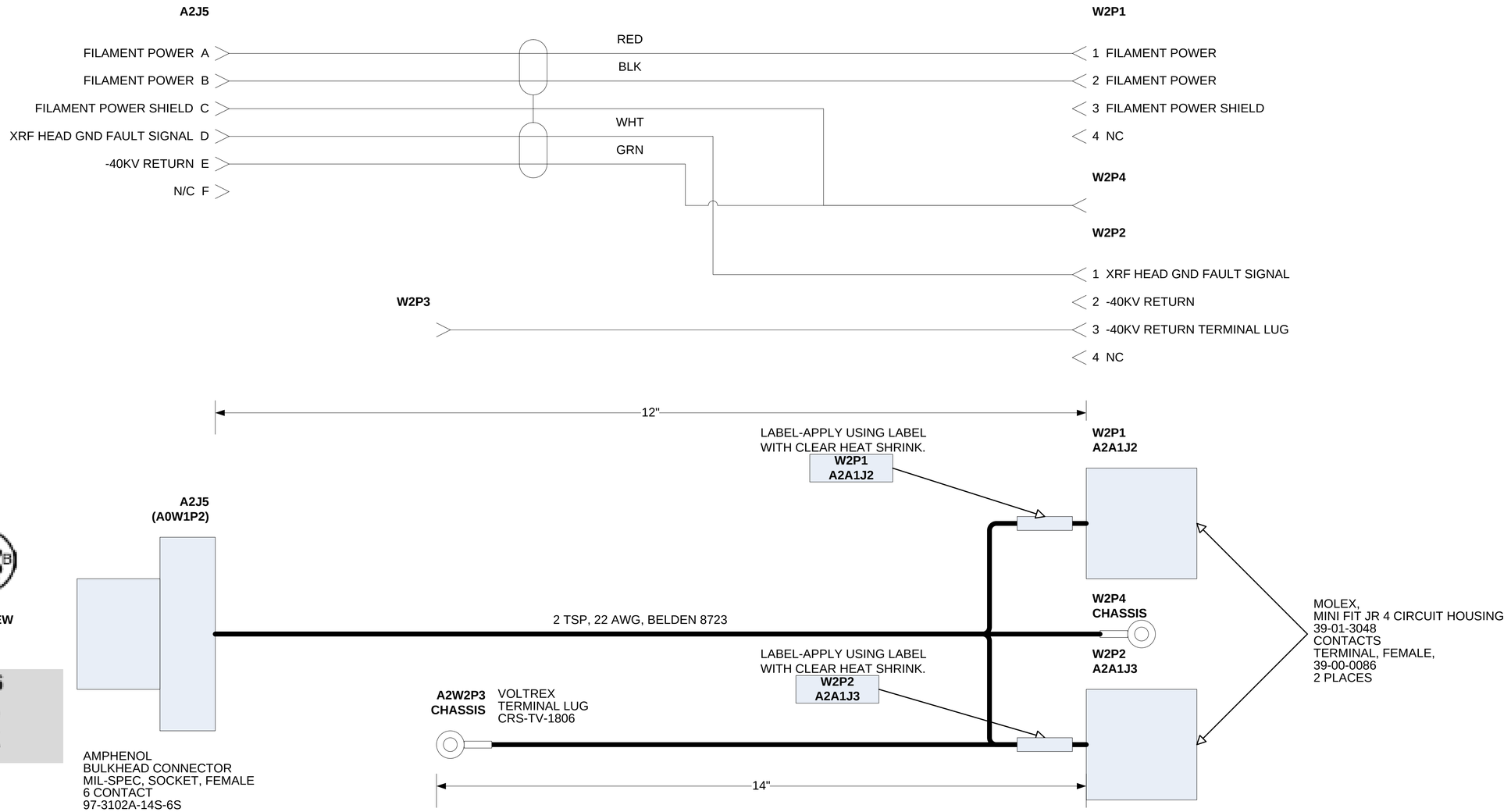


CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON			
DRAWN BY LIGHT	AC POWER, CABLE ASSY A0W8, SYSTEM LEVEL, BOREHOLE XRF PROTOTYPE			
FILENAME BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	SIZE B	CAGE CODE 98514	DWG NO XXXXX	REV
	DATE 23MAY07		SHEET 1 OF 1	

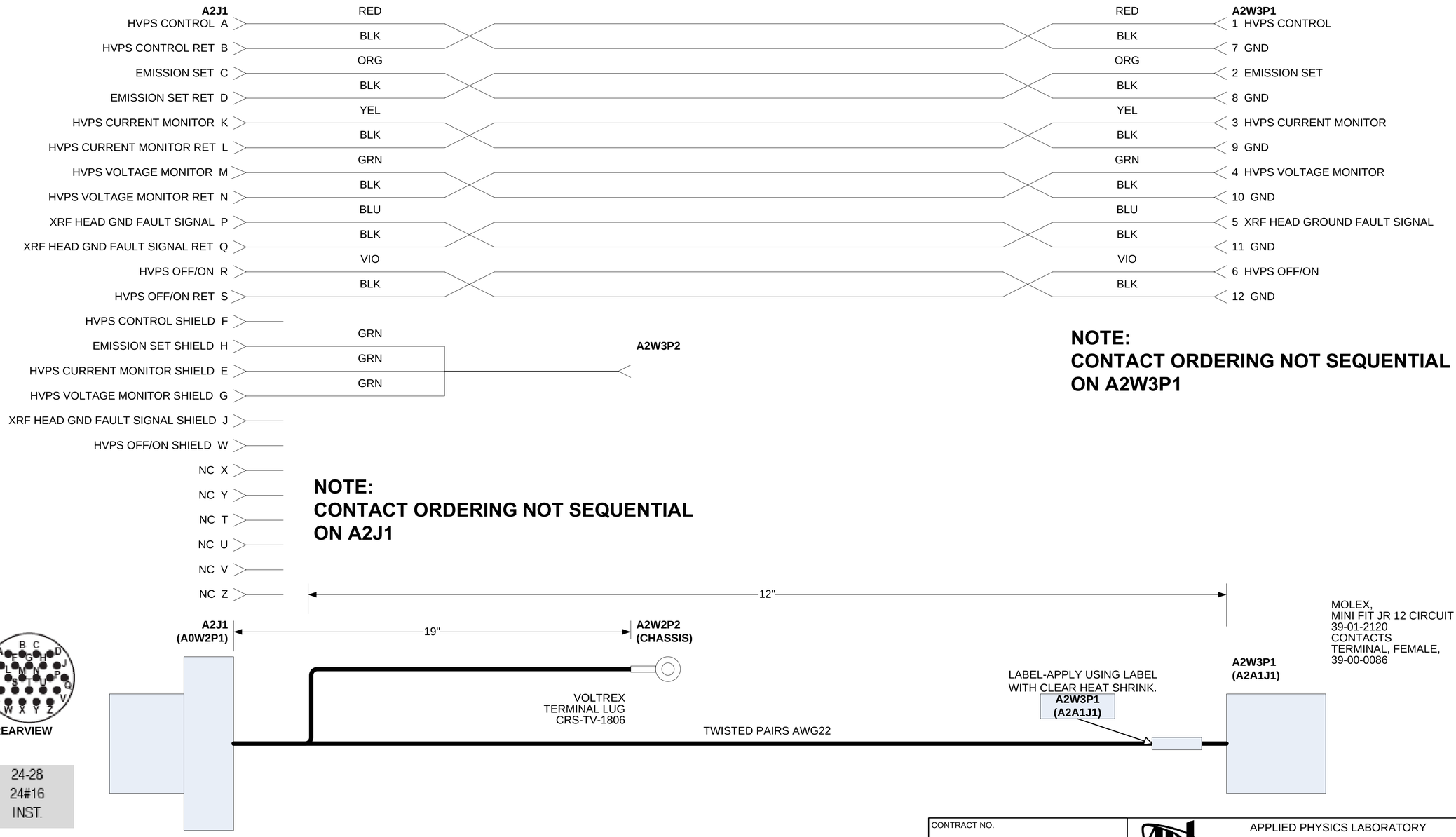


NOTE:
1. POLYCARBONATE ROD DRILLED OUT TO DIAMETER OF THE HIGH VOLTAGE WIRE.
2. SPLICE THE TWO WIRES TOGETHER.
3. FILL VOIDS WITH 5 MINUTE EPOXY.
4. PUT 2 PIECES OF SHIELD BELDEN P/N 92171 OVER HIGH VOLTAGE WIRE. SOLDERED BRAID AT THE SPLICE. TIE BRAID AND NYLON COVERING WITH HEAT SCRINK.
5. TIE SHIELD TO CHASSIS.

CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON
	HIGH VOLTAGE WIRE, CABLE ASSEMBLY A2W2, XRF CONTROL UNIT A0A2, BOREHOLE XRAY PROTOTYPE
DRAWN BY SABIN	
FILENAME BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	SIZE B · CAGE CODE 98514 · DWG NO XXXXX · REV DATE 4JUNE2007 · SHEET 1 OF 1



CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON
	FILIMENT POWER AND XRF HEAD GROUND FAULT SIGNAL, CABLE ASSEMBLY A2W2, XRF CONTROL UNIT A0A2, BOREHOLE XRAY PROTOTYPE
DRAWN BY: SABIN	
FILENAME: BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	SIZE: B · CAGE CODE: 98514 · DWG NO: XXXXX · REV: · DATE: 31MAY2007 · SHEET: 1 OF 1



CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON
	SIGNAL INTERFACE, CABLE ASSEMBLY A2W3, XRF CONTROL UNIT A0A2, BOREHOLE XRF PROTOTYPE
DRAWN BY: SABIN	
FILENAME: BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	SIZE: B · CAGE CODE: 98514 · DWG NO: XXXXX · REV:
	DATE: 31MAY2007 · SHEET: 1 OF 1

A2J2

+5V A
+5V RET B
+5V C
+5V RET D
+15V K
+15V RET L
-15V M
-15V RET N
+15V HVPS P
+15V HVPS RET Q
NC R
NC S
+5V SHIELD F
+5V SHIELD H
+15V SHIELD E
-15V SHIELD G
+15V HVPS SHIELD J
NC W
NC X
NC Y
NC T
NC U
NC V
NC Z

NOTE:
CONTACT ORDERING NOT SEQUENTIAL
ON A2J2

A2W4P2

CENTER CONDUCTOR +5V
OUTSIDE CONDUCTOR +5V RET

YEL
BLK
GRN
BLK
BLU
BLK

A2W4P1

YEL
BLK
GRN
BLK
BLU
BLK

2 +15VA
5 +15VA RET
3 -15VA
6 -15VA RET
1 +15V HVPS
4 +15V HVPS RET

NOTE:
CONTACT ORDERING NOT SEQUENTIAL
ON A2W4P1

LABEL-APPLY USING LABEL
WITH CLEAR HEAT SHRINK.
A2W4P2
(A2A3J3A)

A2W4P2
(A2A3J3A)

MFG WIRE (CUT OFF FROM MFG POWER SUPPLY)

MFG PLUG CUT FROM POWER SUPPLY

A2J2
(A0W3P1)

16"

A2W4P1
(A2A1J4)

LABEL-APPLY USING LABEL
WITH CLEAR HEAT SHRINK.
A2W4P1
(A2A1J4)

TWISTED PAIRS AWG22

MOLEX,
MINI FIT JR 6 CIRCUIT HOUSING
39-01-2060
CONTACTS
TERMINAL, FEMALE,
39-00-0086

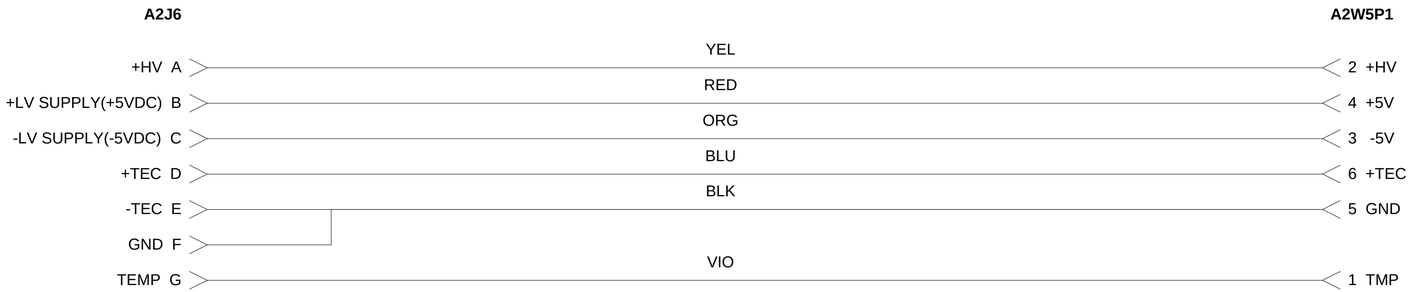
12"

REARVIEW

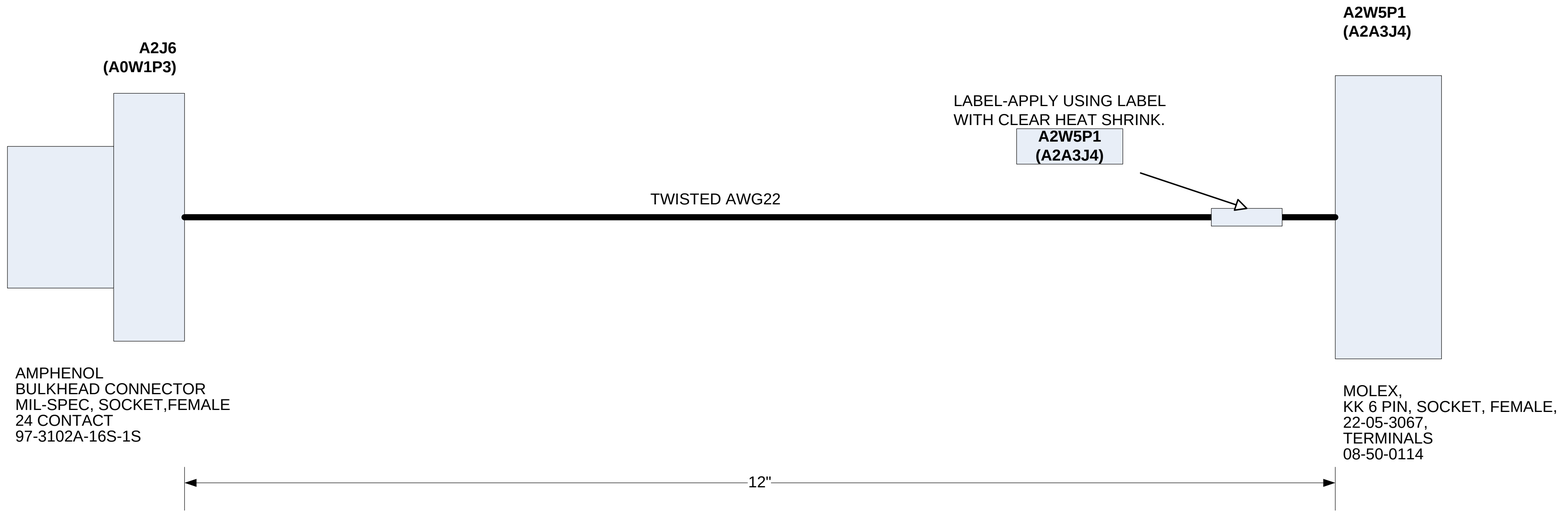
AMPHENOL
BULKHEAD CONNECTOR
MIL-SPEC, JACK, MALE
24 CONTACT
97-3102A-24-28P

24-28
24#16
INST.

CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON
DRAWN BY: SABIN	POWER INTERFACE, CABLE ASSEMBLY A2W4, XRF CONTROL UNIT A0A2, BOREHOLE XRF PROTOTYPE
FILENAME: BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	SIZE: B; CAGE CODE: 98514; DWG NO: XXXXX; REV:
DATE: 31MAY2007	SHEET: 1 OF 1



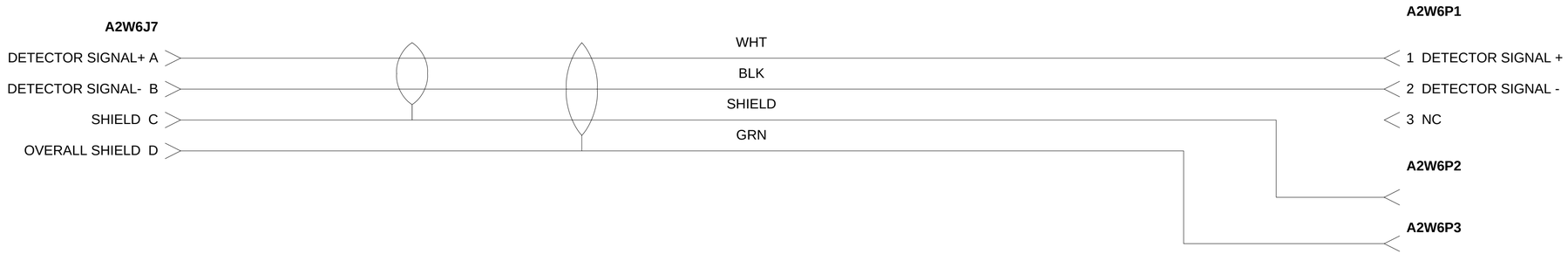
NOTE:
CONTACT ORDERING NOT SEQUENTIAL

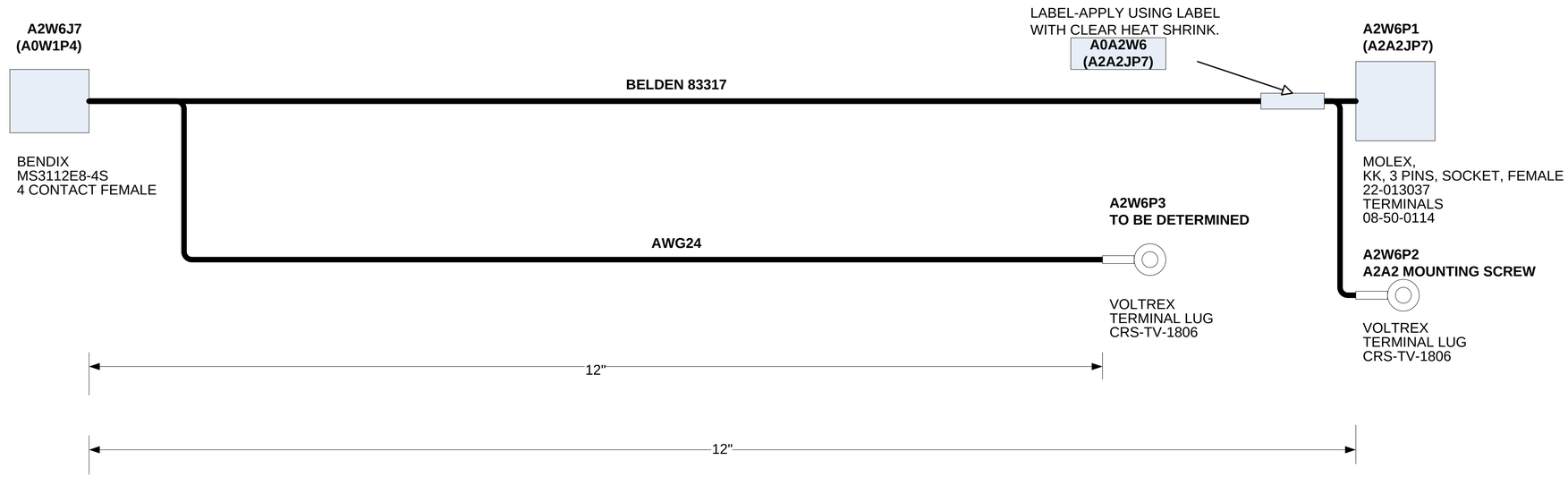


REARVIEW

16S-1
7#16
A

CONTRACT NO.		APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON	
		DETECTOR POWER, CABLE ASSEMBLY A2W5, XRF CONTROL UNIT A0A2, BOREHOLE XRF PROTOTYPE	
DRAWN BY SABIN			
FILENAME BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	SIZE B	CAGE CODE 98514	DWG NO XXXXX / REV
	DATE 31MAY2007		SHEET 1 OF 1





CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON
	DETECTOR SIGNAL, CABLE ASSEMBLY A2W6, XRF CONTROL UNIT A0A2, BOREHOLE XRF PROTOTYPE
DRAWN BY SABIN	
FILENAME BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	SIZE B · CAGE CODE 98514 · DWG NO XXXXX · REV DATE 22AUG2007 · SHEET 1 OF 1

A2W7P1		A2W7P2	
+3.3V	1	1	+3.3V
+5V	2	2	+5V
-5V	3	3	-5V
GND	4	4	GND
GND	5	5	GND
I2C SDA	6	6	I2C SDA
I2C SCL	7	7	I2C SCL
GND	8	8	GND
RS232-RX	9	9	RS232-RX
RS232-TX	10	10	RS232-TX
RS232-CTS	11	11	RS232-CTS
RS232-RTS	12	12	RS232-RTS
GND	13	13	GND
/RESET	14	14	/RESET
USB-	15	15	USB-
USB +	16	16	USB +

A2W7P1
(A2A2JP6)

MFG WIRE

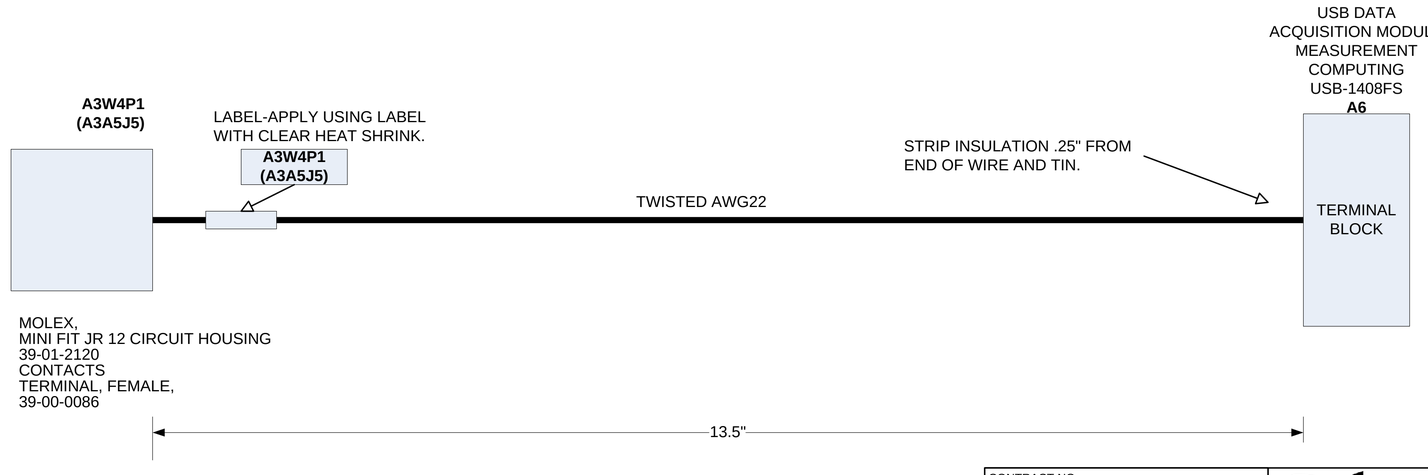
A2W7P2
A2A3J1)

3"

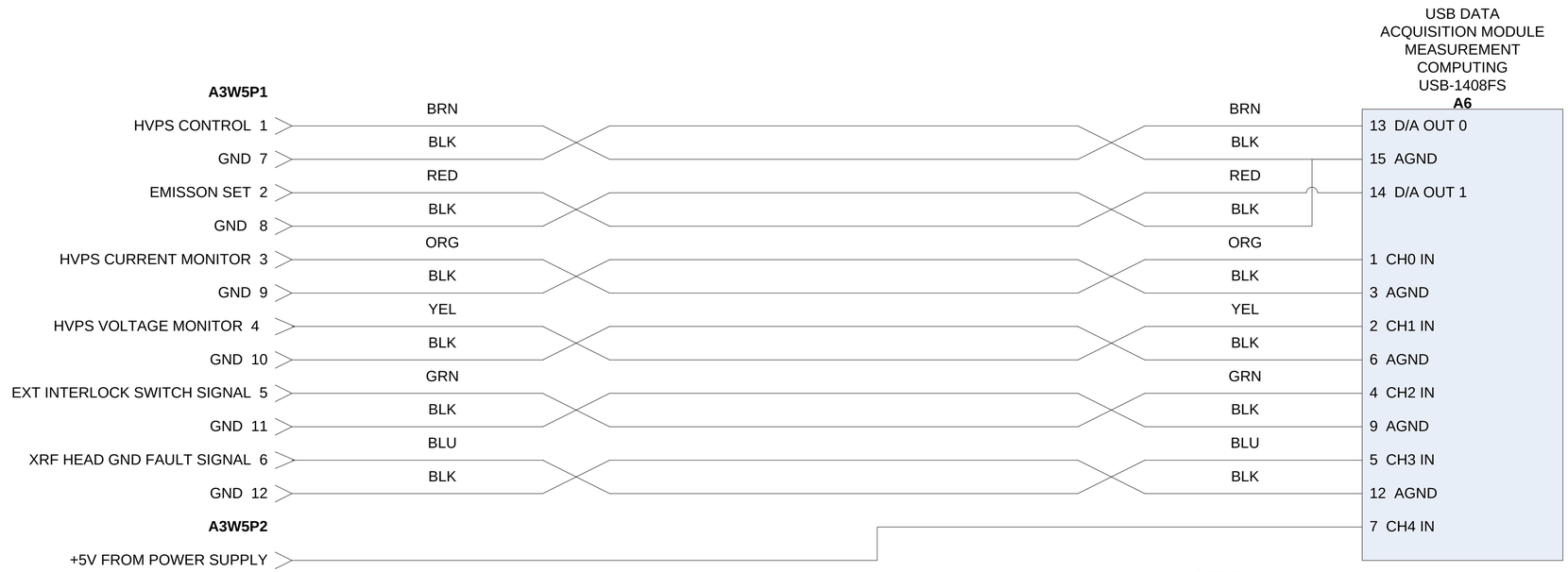
NOTE: NO CONNECTOR IS USED.
CONNECTOR IS PART OF FLEX
CABLE.

CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON
	DP4 TO PC4 INTERFACE, CABLE ASSEMBLY A2W7, XRF CONTROL UNIT A0A2, BOREHOLE XRF PROTOTYPE
DRAWN BY SABIN	
FILENAME BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	SIZE B · CAGE CODE 98514 · DWG NO XXXXX · REV DATE 31MAY2007 · SHEET 1 OF 1

NOTE:
CONTACT ORDERING NOT SEQUENTIAL ON A6

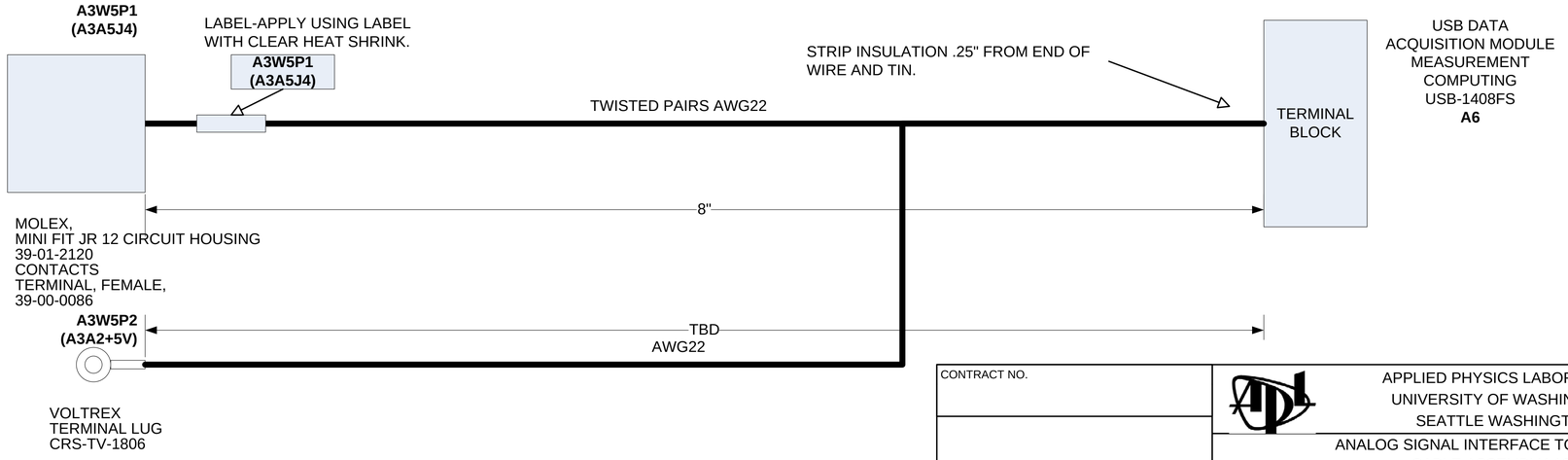


CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON			
	DIGITAL SIGNAL INTERFACE TO USB-1408FS, CABLE ASSEMBLY A3W4, XRF INTERFACE UNIT A0A3, BOREHOLE XRF PROTOTYPE			
DRAWN BY SABIN				
FILENAME BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	SIZE B	CAGE CODE 98514	DWG NO XXXXX	REV
	DATE 31MAY2007		SHEET 1 OF 1	

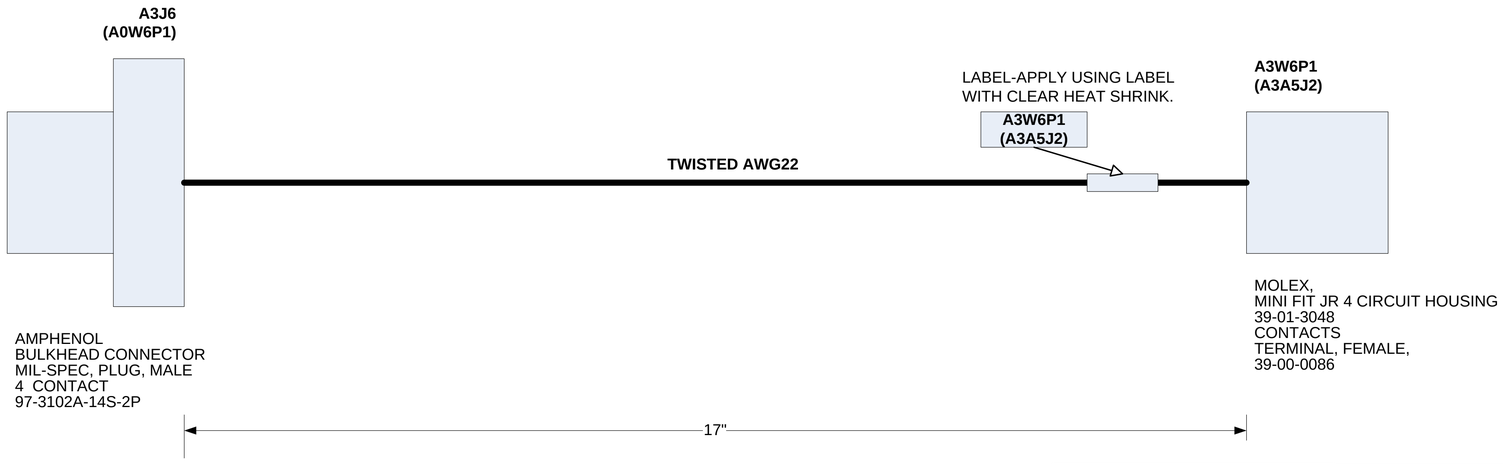


NOTE:
CONTACT ORDERING NOT SEQUENTIAL
ON A3W5P1

NOTE:
CONTACT ORDERING NOT SEQUENTIAL
ON A6



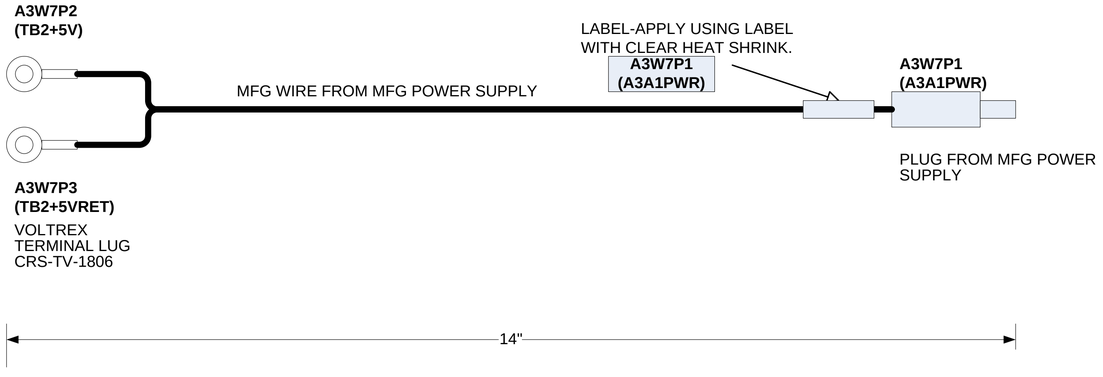
CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON
	ANALOG SIGNAL INTERFACE TO USB-1408FS, CABLE ASSEMBLY A3W5, XRF INTERFACE UNIT A0A3, BOREHOLE XRF PROTOTYPE
DRAWN BY SABIN	
FILENAME BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	SIZE B · CAGE CODE 98514 · DWG NO XXXXX · REV DATE 8JUNE2007 · SHEET 1 OF 1



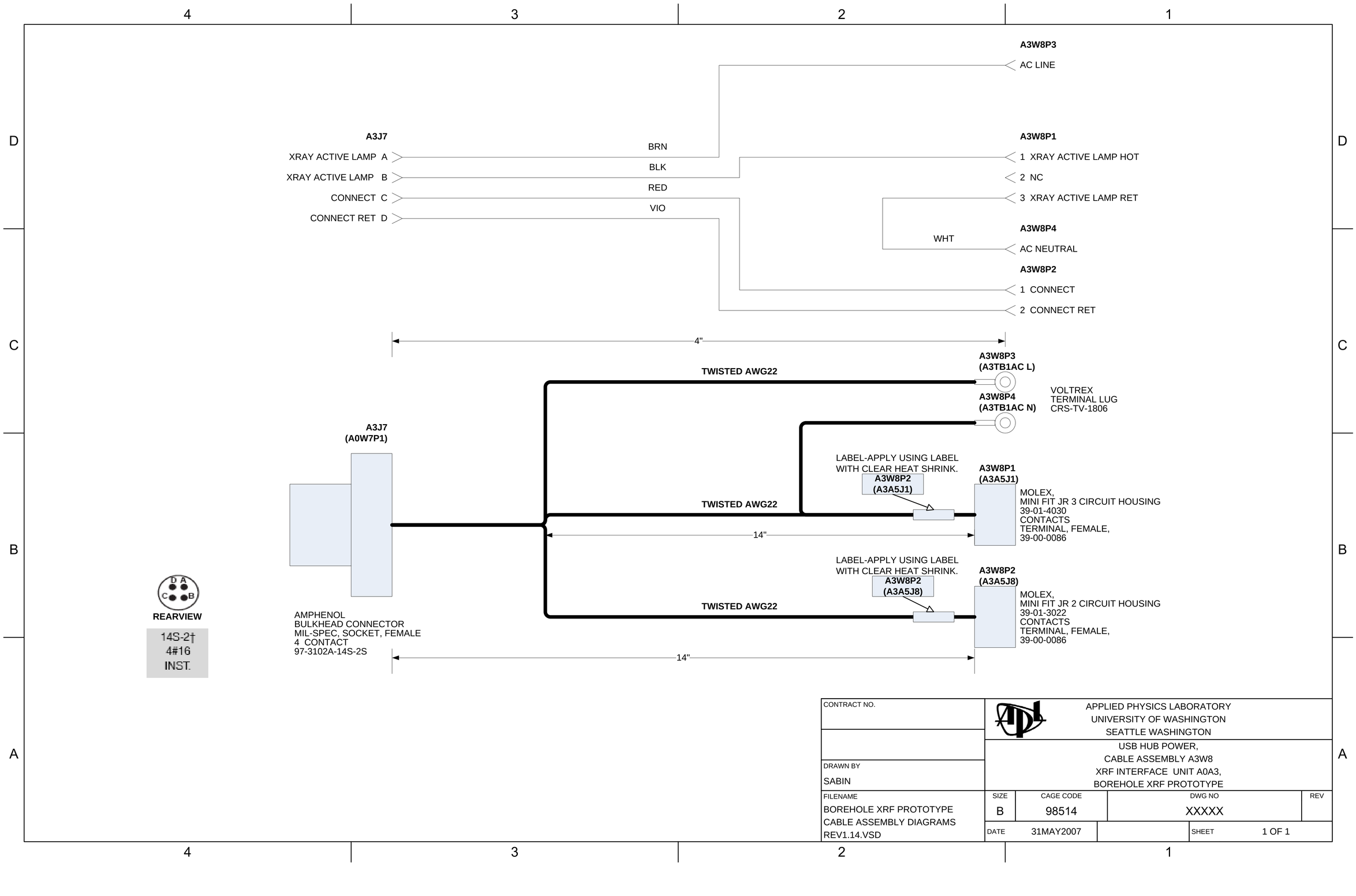
REARVIEW

14S-2†
4#16
INST.

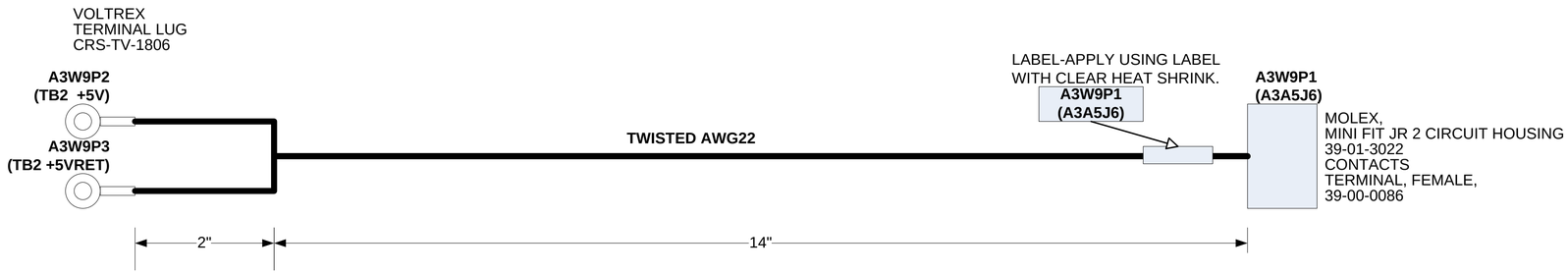
CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON			
	EXTERNAL INTERLOCK SWITCH, CABLE ASSEMBLY A3W6 XRF INTERFACE UNIT A0A3, BOREHOLE XRF PROTOTYPE			
DRAWN BY SABIN				
FILENAME BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	SIZE B	CAGE CODE 98514	DWG NO XXXXX	REV
	DATE 31MAY2007		SHEET 1 OF 1	



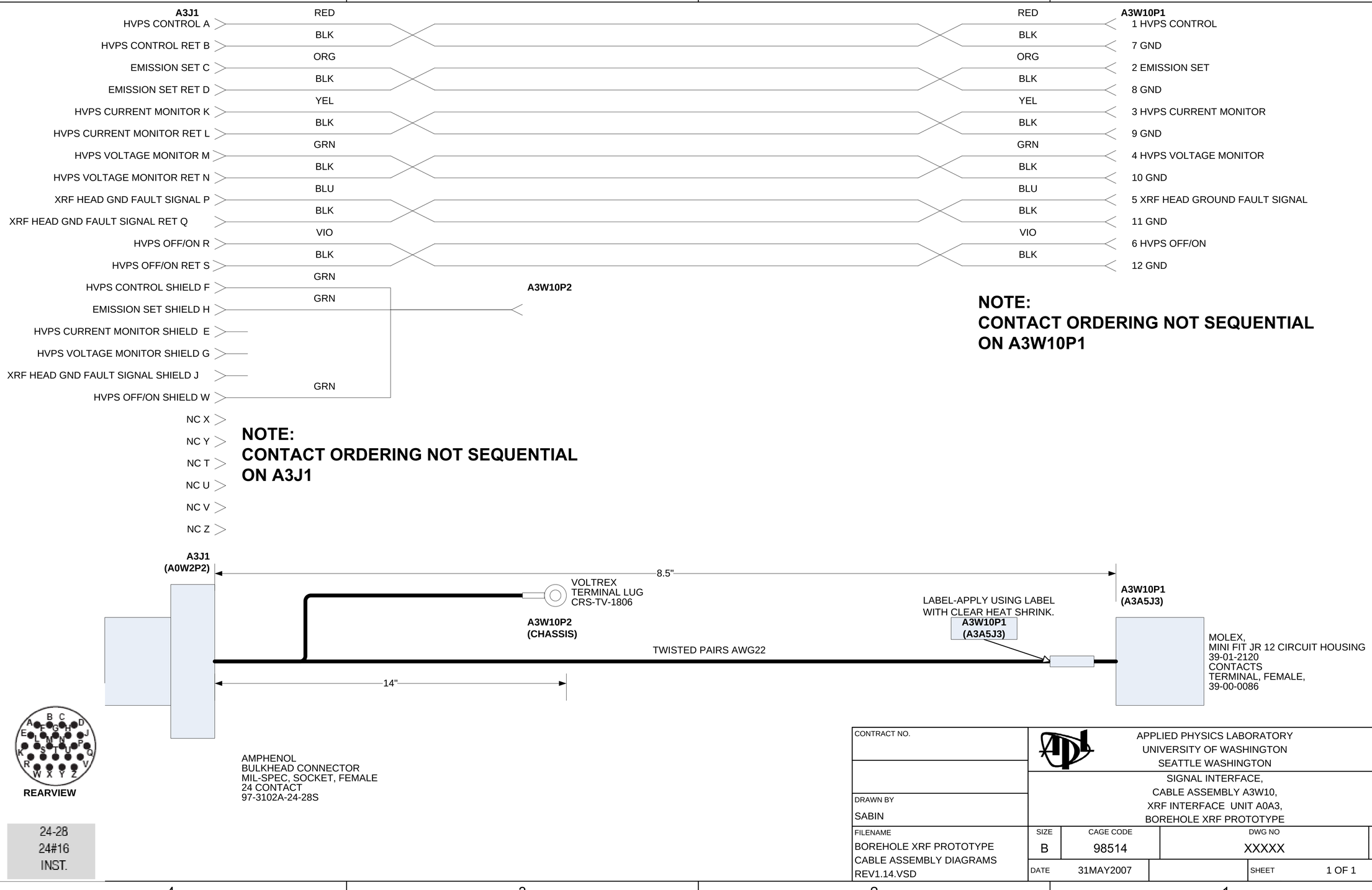
CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON		
	USB HUB POWER, CABLE ASSEMBLY A3W7 XRF INTERFACE UNIT A0A3, BOREHOLE XRF PROTOTYPE		
DRAWN BY SABIN			
FILENAME BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	SIZE B	CAGE CODE 98514	DWG NO XXXXX
	DATE 31MAY2007		SHEET 1 OF 1



CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON			
	USB HUB POWER, CABLE ASSEMBLY A3W8 XRF INTERFACE UNIT A0A3, BOREHOLE XRF PROTOTYPE			
DRAWN BY SABIN	SIZE B	CAGE CODE 98514	DWG NO XXXXX	REV
FILENAME BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	DATE 31MAY2007		SHEET 1 OF 1	

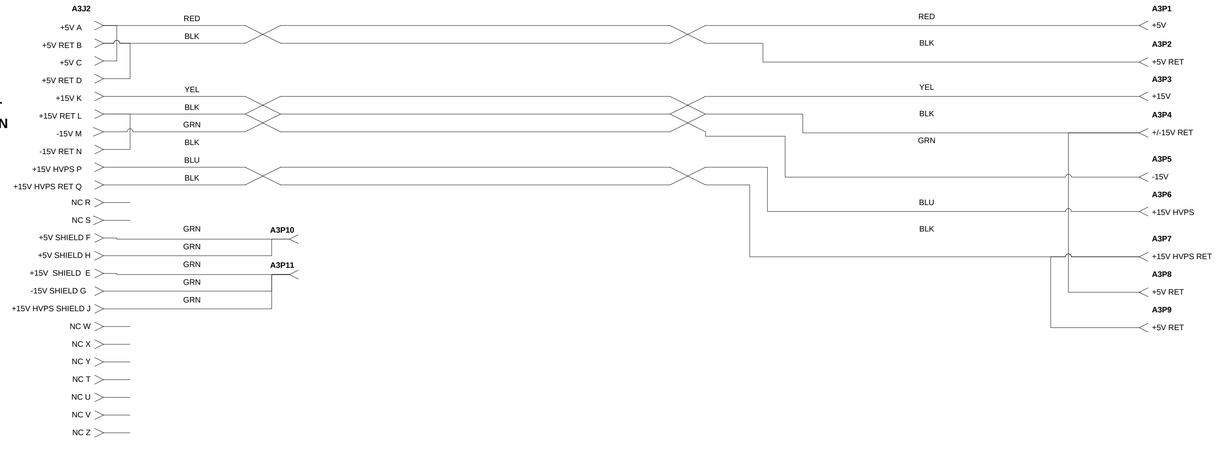


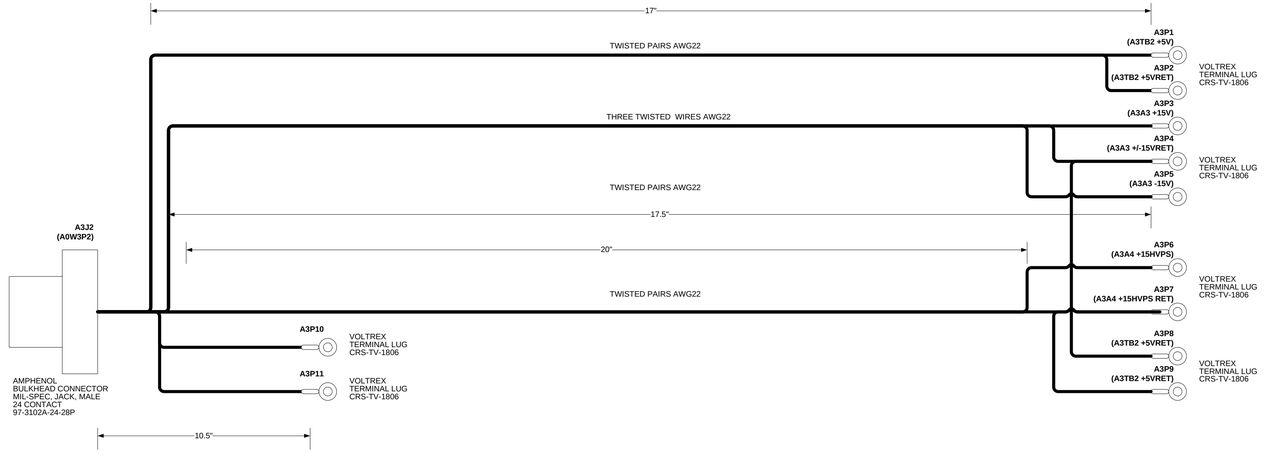
CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON			
	POWER INTERFACE CABLE ASSEMBLY A3W9 XRF INTERFACE UNIT A0A3, BOREHOLE XRF PROTOTYPE			
DRAWN BY SABIN				
FILENAME BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	SIZE B	CAGE CODE 98514	DWG NO XXXXX	REV
	DATE 31MAY2007		SHEET 1 OF 1	



CONTRACT NO.		APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON	
		SIGNAL INTERFACE, CABLE ASSEMBLY A3W10, XRF INTERFACE UNIT A0A3, BOREHOLE XRF PROTOTYPE	
DRAWN BY SABIN			
FILENAME BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	SIZE B	CAGE CODE 98514	DWG NO XXXXX REV
	DATE 31MAY2007		SHEET 1 OF 1

NOTE:
CONTACT ORDERING NOT SEQUENTIAL ON A3J2





24-28
24#16
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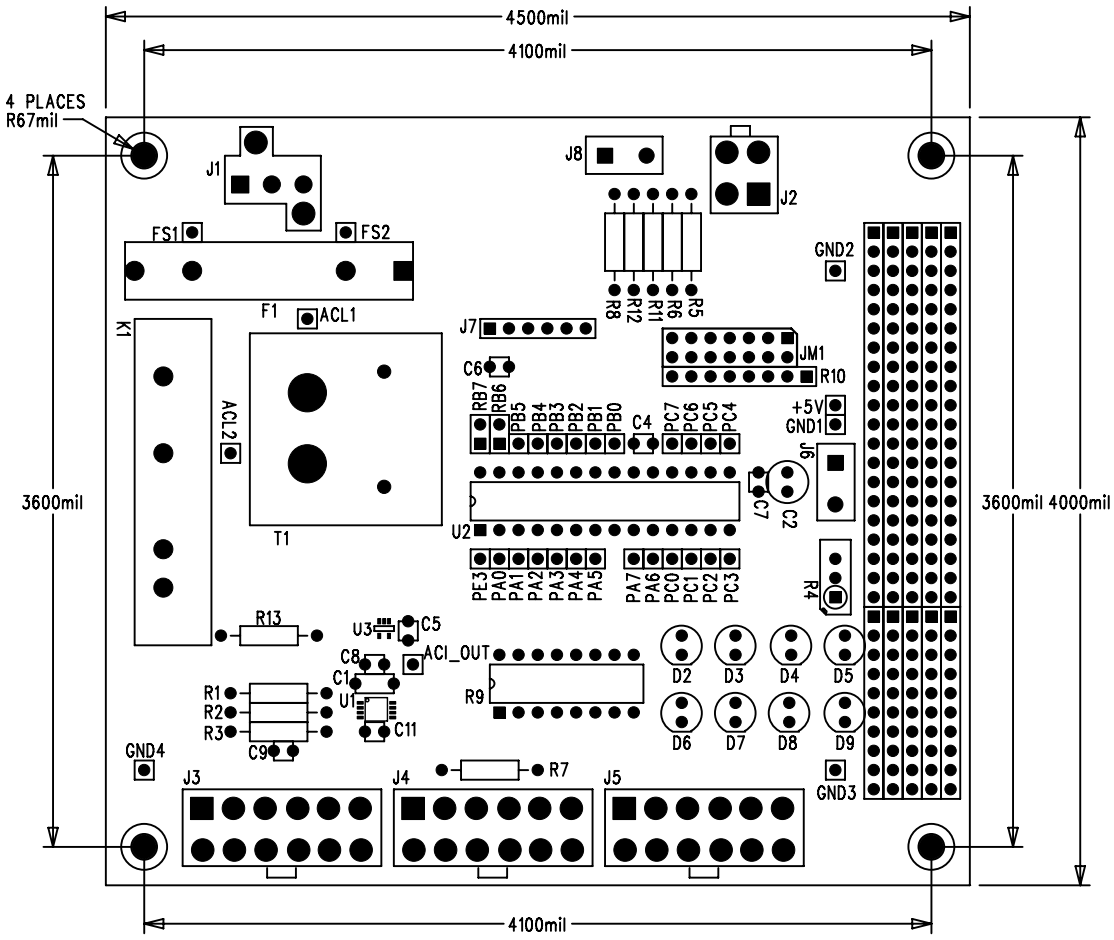
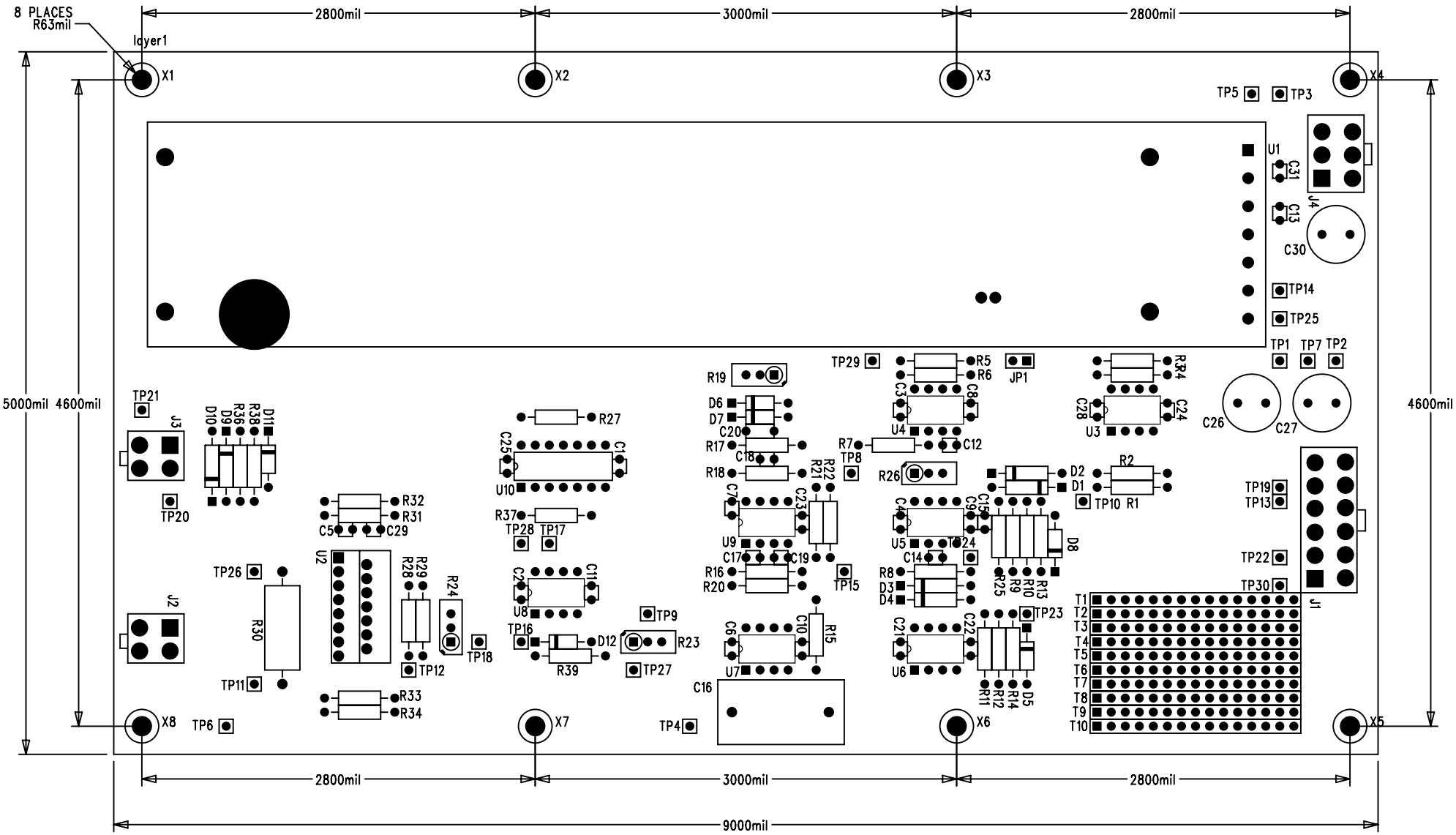
CONTRACT NO.	APPLIED PHYSICS LABORATORY UNIVERSITY OF WASHINGTON SEATTLE WASHINGTON			
	POWER INTERFACE, CABLE ASSEMBLY W11, XRF INTERFACE UNIT A0A3, BOREHOLE XRF PROTOTYPE			
DRAWN BY: SABIN	SIZE: D	CAGE CODE: 98514	DWG NO: XXXXX	REV:
FILENAME: BOREHOLE XRF PROTOTYPE CABLE ASSEMBLY DIAGRAMS REV1.14.VSD	DATE: 31MAY07		SHEET: 1 OF 1	



Safety interlock contol - Mon May 07 08:56:16 2007

HVPS-control.pcb - Mon May 07 08:52:25 2007



Bill Of Materials for Safety interlock control24.sch on Fri May 04 14:05:55 2007

Item	Qty	Reference	Part Name	Part Number
1	2	C7-8	CAP-C320,.01UFD,???	C320C103K5R5CA
2	5	C4-6 C9 C11	CAP-C320,.1UFD,???	C320C104K5R5CA
3	1	C1	CAP-C340,1.0UFD,???	C340C105M1U5TA
4	1	C2	CAP-T35X,47ufd,???	T350J476K016AT
5	1	J2	CON-MOLEX-CGRID-4P-P	39-28-1043
6	2	J3-J5	CON-MOLEX-MINIFITJR-12P-S	39-31-1123
7	2	J6 J8	CON-MOLEX-MINIFITJR-VT-2P	39-28-1023
9	1	J1	CON-MOLEX-MINIJR-3S	39-30-2037
10	2	RB6-7	CON-SIP-2P	
11	1	J7	CON-SIP-6P	
12	33	+5V ACI_OUT ACL1-2 FS1-2 GND1-4 PA0-7 PB0-5 PC0-7 PE3	CON\SIP\1P	
13	1	T1	CSE187	CSE187L
14	1	F1	FUSE_PCB_1250,1A	1020071H
15	1	JM1	JMP14	
16	8	D2-9	LED	SSL-LX3044ID-12V
17	1	U3	LMV771	LMV771MG
18	1	U1	LTC1966	LTC1966CMS8
19	1	U2	PIC16F882/883/886	PIC16F886USE 28 PIN SOCKET
20	1	K1	RELAY-CRYDOM-MCX-S	MCX240D5
21	4	R2-3 R11-12	RES-1/4W,100k	
23	4	R5-6 R8 R13	RES-1/4W,10k	
24	1	R1	RES-1/4W,1k	
25	1	R7	RES-1/4W,20k	
26	1	R9	RES-DIP168RES,270	4116R-1-271LF
27	1	R10	RES-SIP8P7RG,220k	4308R-101-224
28	1	R4	VRES-TOP-ADJ	NOT INSTALLED

Bill Of Materials for Xray2-19.sch on Tue Apr 17 13:27:58 2007

Item	Qty	Reference	Part Name	Part Number
1	1	U8	AD633	AD633AN
2	1	U10	AD7512D1	AD7512DIJNZ
3	22	C1-13 C15 C21-25 C28-29 C31	CAP-C320,.1ufd,???	C320C104K5R5CA
4	1	C14	CAP-C320,100pfd,???	C320C101J2G5TA
5	2	C18-19	CAP-C320,33pfd,???	C320C330J2G5TA
6	1	C17	CAP-C320,68pfd,???	C320C680J2G5TA
7	1	C20	CAP-C340,1ufd,???	B32529C105J
8	1	C16	CAP-PANA-.690,4.7UFD	ECQ-E2475KB
9	3	C26-27 C30	CAP-T35X,100ufd,???	T350M107K020AT
10	1	J1	CON-MOLEX-MINIJR-12S	39-29-3126
11	2	J2-3	CON-MOLEX-MINIJR-4S	39-29-3046
12	1	J4	CON-MOLEX-MINIJR-6S	39-29-3066
13	30	TP1-30	CON\SIP\1P	STOCK
14	6	D1-4 D9-10	DIODE	1N4148
15	1	JP1	JMP-2P	DO NOT INSTALL
16	5	U3-7	LF356J	LF356N
17	1	U2	LM1876	LM1876T/NOPB
18	1	U9	LM1458J	LM1458N
19	1	R7	RES-1/4W,1.0M	CFR-25JB-1M0
20	8	R1-4 R13-14 R21 R39	RES-1/4W,100k	CFR-25JB-100K
21	6	R9 R11-12 R18 R27 R38	RES-1/4W,10k	CFR-25JB-10.0K
22	6	R25 R28-29 R32 R34 R37	RES-1/4W,1k	CFR-25JB-1.00K
23	3	R22 R31 R33	RES-1/4W,20k	CFR-25JB-20.0K
24	1	R10	RES-1/4W,27.4k	CFR-25JB-27.4K
25	1	R5	RES-1/4W,3.3M	CFR-25JB-3M3
26	1	R20	RES-1/4W,330k	CFR-25JB-330K
27	1	R6	RES-1/4W,4.7M	CFR-25JB-4M7
28	3	R8 R16-17	RES-1/4W,470k	CFR-25JB-470K
29	1	R36	RES-1/4W,49.9k	CFR-25JB-49.9K
30	1	R15	RES-1/4W,51k	CFR-25JB-51.1K
31	1	R30	RES-1W,1,1W	5073NW1R000J12AFX
32	1	U1	UV-40A12	40A12-N4
33	2	R23-24	VRES-TOP-ADJ,10k	3296W-1-103
34	1	R19	VRES-TOP-ADJ,250k	3296W-1-254
35	1	R26	VRES-TOP-ADJ,25k	
36	1	D11	ZENER-DIODE,4.7v	1N5230B
37	1	D8	ZENER-DIODE,5.1v	1N5231B
38	4	D5-7 D12	ZENER-DIODE,6.2v	1N5234B

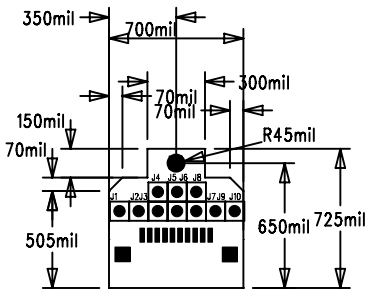
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

APPLIED PHYSICS LABORATORY	
CONTRACT NO.	
DIRECTOR	
PROJ ENGR	SABIN
ENGINEER	
CHECKED:	
DRAWN:	SABIN
APPLICATION DATA	
NEXT ASSY.	USED ON

APPLIED PHYSICS LABORATORY
UNIVERSITY OF WASHINGTON
SEATTLE WASHINGTON

XRF DETECTOR INTERFACE BOARD, A0A1A3, SCHEMATIC, XRF HEAD, BOREHOLE XRF PROTOTYPE

SIZE:	CODE:	DRAWING NO:
	98514	
DATE:	17 APR 2007	



XRF head interface boar - Mon May 07 08:46:58 2007

```
/************************************************************
*                                    XRF safety controller program                    *
*                                                  5/1/2007                                                  *
*                                            Author Peter Sabin                                          *
*                                                                                                                                  *
*       This progam takes input from the XRF hardware and                *
*checks the status of the hardware. It then will send this      *
*status information to the host computer. It will also make     *
*a determination if the XRAY HVPS can be turned on. If all      *
*the hardware is in the non-error condition and the host        *
*computer send a signal to turn on the XRAY HVPS the            *
*controller will turn on the XRAY lamp and the XRAY HVPS.       *
*The controller will constanly monitor the hardware for         *
*errors conditions and shuts off the XRAY HVPS if there is a*
*hardware error condition.                                                                        *
*                                                                                                                                  *
*Microcontroller used is the PIC16F886                                                *
*                                                                                                                                  *

* The PIC16F886 has the following port assignments                    *
*       Port A                                                                                                                  *
*               Bit0    Analog  Monitors HVPS current                                *
*               Bit1    Analog  Monitors XRAY warnig lamp                            *
*               Bit2    Analog  Monitors XRF head ground fault                  *
*               Bit3    Analog  Monitors External interlock Sw                  *
*               Bit4    Digital Monitors XRAY On/Off signal                          *
*               Bit5    Analog  Monitors on board potentiometer                 *
*               Bit6    Digial  Monitors Ext.interlock connection               *
*               Bit7    digital Monitors XRAY lamp connection                   *
*                                                                                                                                  *
*       Port B                                                                                                                  *
*               Bit0    Digital Status output for Microcontroller               *
*               Bit1    Digital Status output for lamp connection               *
*               Bit2    Digital Status output for lamp status                   *
*               Bit3    Digital Status output for HVPS current                  *
*               Bit4    Digital Status output for XRF head gnd fault*
*               Bit5    Digital Status output for interlock sw fault*
*               Bit6    Digital Status output for interlock sw conn             *
*               Bit7    Digital Status output for interlock sw                  *
*                                                                                                                                  *
*       Port C                                                                                                                  *
*               Bit0    Digital output Control bit for HVPS                          *
*               Bit1    Digital Output Control bit for XRAY lamp                *
*               Bit2    Digital Not used                                                                *
*               Bit3    Digital Not used                                                                *
*               Bit4    Digital Not used                                                                *
*               Bit5    Digital Not used                                                                *
*               Bit6    Digital RS232 TX Output                                                *
*               Bit7    Digital RS232 RX Input                                                 *
*                                                                                                                                  *
*       Port E                                                                                                                  *
*               Bit3    Used for programming                                                   *
************************************************************/

/************************************************************
*       Include files                                                                                                  *
************************************************************/

#include <16F886.h>
#include <XRF safety controller1.h>

/************************************************************
*       Fuses                                                                                                                  *
*               INTRC_IO        Internal RC osc RA6/RA7 set for IO                   *
*               NOLVP           No low voltage programming on RB3                    *
*               WDT                     Enable watch dog timer                                          *
*               NOIESO          No int/ext oscillator switchover                     *
*               NOPROTECT       Do not protect program memory                        *
*               NOCPD           Do not protect EEprom                                        *
*               PUT                     Use power up timer for restarts                      *
************************************************************/

#fuses INTRC_IO,NOLVP,WDT,NOIESO,NOPROTECT,NOCPD,PUT

/************************************************************
*       Set clock speed to 4Mhz                                                                         *
************************************************************/

#use delay(clock=4Mhz)
```

```
/*********************************************************
*       Set RS232 interface used for testing uses RC6/RC7              *
*********************************************************/

#use rs232(baud=9600,uart1)

/*********************************************************
* setup ports to use TRIS command                                       *
*********************************************************/

#use fast_io(a)
#use fast_io(b)
#use fast_io(c)


/*********************************************************
* Subroutines                                                           *
*********************************************************/

/*********************************************************
* PIC_INITIALIZE                                                        *
* Routine to ports A,B and C, Status bits, WDT and timer1       *
*********************************************************/
void PIC_INITIALIZE()
        {
        printf("Pic initializing\n");
        output_b(0x0fe);                // set PortB bits to 1
                                                //except bit 0
        output_c(0x00);                 // set PortC bits to 0

        set_tris_a(0x0ff);              //set all PortA to inputs
        set_tris_b(0x00);               //set all PortB to outputs
        set_tris_c(0x0dc);              //set PortC bits 0,1 and 6 output
                                                //all others as inputs

        setup_wdt(WDT_DIV_8192);//set WDT for about 268ms rate

        setup_timer_1(T1_INTERNAL|T1_DIV_BY_8);
                                                //setup timer1, output is about
                                                //524ms
        setup_adc_ports(sAN0|sAN1|sAN2|sAN3|sAN4);
                                                //set up port A bits 0,1,2,3and 5
                                                //as ADC ports
        setup_adc(ADC_CLOCK_DIV_8);
                                                // use FOSC/8 adc clock
        }

/*********************************************************
* CHECK_EXTERNAL_INTERLOCK_SWITCH                                       *
* Routine to check external interlock switch for the            *
* following conditions:                                                 *
* 1. Switch not connected(portA bit 6)                                  *
* 2. Switch is shorted or is open(portA bit 3)                  *
*                                                                                                               *
* PortB bit 5,6 and 7 will show the status of the interlock     *
* switch as follows:                                                    *
* bit5 = failure of interlock switch                                    *
* bit6 = connection fault                                               *
* bit7 = either short or open interlock switch                  *
*********************************************************/

void CHECK_EXTERNAL_INTERLOCK_SWITCH()
        {
        long value;
        printf("Checking external interlock switch\n");
        if((input(INTERLOCK_SWITCH_CONNECT))==0)
                                                //check for connection
                {
                output_high(INTERLOCK_SWITCH_FAULT_STATUS);
                output_high(INTERLOCK_SWITCH_CONNECT_STATUS);
                }
        else output_low(INTERLOCK_SWITCH_CONNECT_STATUS);

        set_adc_channel(INTERLOCK_SWITCH_SIGNAL);
                                                //check for short or open
        delay_us(10);                           //read value on ADC3
        value=read_adc();                       //if <.5v or >3.33v then
                                                //switch is either shorted or open
```

```
        printf("Interlock switch =%4Lu\n",value);

        if(value<=100||value>=600)
                {
                output_high(INTERLOCK_SWITCH_STATUS);
                output_high(INTERLOCK_SWITCH_FAULT_STATUS);
                }
        else
                {
                output_low(INTERLOCK_SWITCH_FAULT_STATUS);
                output_low(INTERLOCK_SWITCH_STATUS);
                }
        }

/*********************************************************
* CHECK_XRF_HEAD_GND                                                    *
* Routine that checks the XRF head ground connection.           *
* (PortA bit2,RA2)                                                      *
* If XRF head ground signal is less than 2.5v(512) the          *
* system is OK.                                                         *
* Above this value and the ground is cut.                               *
*********************************************************/

void CHECK_XRF_HEAD_GND()
        {
        long value;
        printf("Checking XRF ground fault.\n");

        set_adc_channel(XRF_HEAD_GROUND_FAULT_SIGNAL);
                                                //check voltage on ADC2
        delay_us(10);                           //this is the ground voltage
        value=read_adc();
        printf("XRF head voltage =%4Lu \n", value);

        if(value<512) output_low(XRF_HEAD_GROUND_FAULT_STATUS);
        else output_high(XRF_HEAD_GROUND_FAULT_STATUS);
        }

/*********************************************************
* CHECK_HVPS_CURRENT                                                    *
* Routine to test the HVPS current                                      *
* Uses current monitor PortA bit 0 (RA0)                                *
* If the current is above a value determined by measurement     *
* then a timer starts and to see if the current stays high      *
* for 5 seconds. If the current high for over 5 seconds         *
* then set fault XRAY_HVPS_CURRENT_STATUS (PortB bit4)          *
*********************************************************/

void CHECK_HVPS_CURRENT()
        {
        long value;
        printf("Checking HVPS current.\n");

        set_adc_channel(XRAY_HVPS_CURRENT_SIGNAL);
                                                        //check AD0 for HVPS current
        delay_us(10);
        value=read_adc();
        printf("HVPS current =%4Lu \n", value);

        if(value>MAX_CURRENT)                   //check if counter timer1 int
                {                                               //is started if not start.
                if(CURRENT_TIMER>0)                     //0 not started >0 started
                        {
                        if(CURRENT_TIMER>MAX_TIMER_VALUE)
                                {                               // HVPS high current exceeded time
                                output_high(XRAY_HVPS_CURRENT_STATUS);
                                                        //max count done stop timer1
                                disable_interrupts(GLOBAL);
                                disable_interrupts(INT_TIMER1);
                                CURRENT_TIMER=0;
                                }
                        }
                else
                        {
                        enable_interrupts(INT_TIMER1);  //not started so start
                        enable_interrupts(GLOBAL);
                        }
                }
        else
```

```
                {
                disable_interrupts(GLOBAL);
                disable_interrupts(INT_TIMER1);
                CURRENT_TIMER=0;
                output_low(XRAY_HVPS_CURRENT_STATUS);
                }
        }

/*********************************************************
* XRAY_ACTIVE_LAMP_FAULT                                                 *
* Routine to check if the lamp is drawing current and to see*
* if the lamp is connected                                               *
* Uses PortA bit1(RA1)  current monitor                          *
* Uses PortA bit7       lamp connection                          *
* If lamp not connected then set fault flag                *
* XRAY_ACTIVE_LAMP_CONNECT_STATUS(PortB bit 1)             *
* If the current is the nominal value then clear fault          *
* flag XRAY_ACTIVE_LAMP_CURRENT_STATUS(PortB bit2)         *
*********************************************************/

void XRAY_ACTIVE_LAMP_FAULT()
        {
        long value;
        printf("Checking Active Lamp.\n");
        if((input(XRAY_ACTIVE_LAMP_CONNECT))==1)
                {
                output_low(XRAY_ACTIVE_LAMP_CONNECT_STATUS);
                set_adc_channel(XRAY_ACTIVE_LAMP_CURRENT_SIGNAL);
                delay_us(10);
                value=read_adc();
                printf("Lamp current =%4Lu\n", value);

                if(value<LAMP_CURRENT_MIN||value>LAMP_CURRENT_MAX)
                        {
                        output_high(XRAY_ACTIVE_LAMP_STATUS);
                        }
                else output_low(XRAY_ACTIVE_LAMP_STATUS);
                }
        else
                {
                output_high(XRAY_ACTIVE_LAMP_CONNECT_STATUS);
                output_high(XRAY_ACTIVE_LAMP_STATUS);
                }

        }

/*********************************************************
* CHECK_ON/OFF_XRAY_CONTOL_CMD                                   *
* Routine used during error conditiond to make sure the         *
* user turns off the XRF and then we can continue          *
* Uses PortA bit4                                                        *
*********************************************************/

void CHECK_ON_OFF_XRAY_CONTROL_CMD()
        {
        while((input(XRAY_CONTROL_CMD))==1)
                {
                printf("waiting\n");
                }
        }
/*********************************************************
* TIMER1_ISR                                                             *
* Routine for the timer1 ISR                                     *
* Add one to counter when timer1 interrupt occurs          *
*********************************************************/
#INT_TIMER1
void TIMER1_ISR()
        {
        CURRENT_TIMER++;
        }

/*********************************************************
* Main subroutine                                                        *
* 1. Check to see if boot was caused by the watchdog.           *
* If the watchdog caused the boot then set PortB bit0           *
* and stop the program.                                                  *
* 2. Initialize the PIC                                                  *
* 3. Check the fault hardware                                    *
* 4. Check to see if the user wants to turn on the XRF.         *
```

```
* 5. If true then turn on the XRF.                                                    *
* 6. Continue checking until a fault occurrs or the user       *
* off the XRF.                                                                                    *
************************************************************/
void main()
        {
        int flag_status;
        if(restart_cause()==WDT_TIMEOUT)
                {
                while(1)
                        {
                        set_tris_b(0x0);
                        output_high(XRAY_CONTROLLER_FAIL_STATUS);
                        }
                }

        restart_wdt();
        PIC_INITIALIZE();
        restart_wdt();
        while(1)
                {
                restart_wdt();
                CHECK_EXTERNAL_INTERLOCK_SWITCH();
                CHECK_XRF_HEAD_GND();
                CHECK_HVPS_CURRENT();
                if((input(XRAY_CONTROL_CMD))==1)
                        {
                        output_high(XRAY_ACTIVE_LAMP_CONTROL);
                        delay_ms(10);
                        XRAY_ACTIVE_LAMP_FAULT();
                        flag_status=input_b();
                        if(flag_status==0)
                                {
                                output_high(XRAY_HVPS_CONTROL);
                                }
                        else CHECK_ON_OFF_XRAY_CONTROL_CMD();
                        }
                else
                        {
                        output_low(XRAY_HVPS_CONTROL);
                        output_low(XRAY_ACTIVE_LAMP_CONTROL);
                        }
                }
        }
```